Distributed Signal and Noise Modeling of Millimeter Wave Transistor Based on CMOS Technology

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Abstract **─** This paper presents a complete distributed transmission line signal and noise modeling of millimeter wave CMOS transistor. In this model, the MOSFET transistor is considered as a three-coupled active transmission line structure, exciting by the noise equivalent sources distributed on its conductors. According to the transmission line theory, closed form expressions of the signal and noise parameters for a high frequency CMOS transistor are derived as the function of device width. By using the proposed model, the scattering and noise parameters of a 130 nm MOSFET are computed over a frequency range up to 100 GHz. The results obtained by this approach is compared with the lumped elements model and verified by the simulation results of Cadence SpectreRF simulator.

Index Terms **─** Cadence, CMOS transistor, coupled active transmission line, distributed transmission line model, lumped MOSFET model, millimeter wave.

I. INTRODUCTION

With the advancement in CMOS technology, the MOS transistors are scaled down into deep submicron regime with higher transit frequency. The high frequency capabilities of MOSFETs are very attractive for millimeter (mm) wave circuit design due to their ability of chip integration, low cost and low power consumption [1]. As the operating frequency of MOSFETs increases to the mm-wave range, the width of the device becomes comparable to the wave length. In such cases, the distributed transmission line effect needs to be considered accurately, in device modeling.

In previous works [2], [3] and [4] the distributed transmission line effect along the gate width has been studied. In these distributed models, the gate width is divided into finite number of slices that are connected together by using of series of scaled gate resistor. In [2], the thermal noise due to the gate resistance was incorporated in the model. In [3], MOSFET distributed model of [2] is improved by including the distributed charging resistance and the induced gate noise along the gate width. Nevertheless, in these studies only distributed behavior of transistor along gate electrode width is modeled and other electrodes are ignored. Furthermore, the effects of the transmission line capacitances and inductances along the device width are not considered.

In this paper, a complete distributed transmission line signal and noise modeling of mm-wave MOSFET transistor that considered it as the excited three-coupled active transmission line structure, exciting by noise equivalent sources distributed on the conductors, is presented. The details of the proposed model are described in the next section. In Section III, the introduced approach is used in signal and noise modeling of 130 nm MOSFET and its results are discussed and compared with lumped and previous distributed models. Finally, the paper is concluded in the last section.

II. DISTRIBUTED MM-WAVE MOSFET MODELING

A. Distributed signal analysis

The proposed distributed model considers the MOSFET as three-coupled active transmission line, is shown in Fig. 1 (a). In this model, the device width is divided into an infinity number of segments, while each segment is separated into parallel intrinsic and extrinsic contributions. The parameters G_m, C_{gs}, C_{ds}, C_{gd}, R_g, R_d and R_{ds} taken together are referred to as the intrinsic elements and standard BSIM4 model [5] is employed to compute them. BSIM4 is the physical MOSFET model supplied with Berkeley SPICE and models the channel current by using a complete single equation for both linear and saturation regions as:

$$I_{ds} = \frac{V_{dseff} I_{ds0}(V_{dseff})}{V_{dseff} + R_{ds} I_{ds0}(V_{dseff})}\left(1+\frac{V_{ds}-V_{dseff}}{V_A}\right)\left(1+\frac{V_{ds}-V_{dseff}}{V_{ASCBE}}\right), \quad (1)$$

and transistor conductance G_m can be obtained as:

$$G_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=\text{Const.}}. \quad (2)$$

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The detailed equations of I_{ds0}, V_{dseff}, V_{ASCBE} and V_A have been given in [5]. In this model, capacitances are derived from the charges to ensure charge conservation. The space charge of a MOS structure consists of three fundamental components: the charge on the gate electrode, Q_G, the charge in the bulk depletion layer, Q_B, and the mobile charge in the channel region, Q_{INV}. Generally, the following relationship holds in a MOSFET:

$$Q_G + Q_{INV} + Q_B = 0, \tag{3}$$

and

$$Q_{INV} = Q_D + Q_S, \tag{4}$$

where Q_D and Q_S are the channel associated with the drain node and the source node, respectively. Capacitance between any two of the four terminals (gate, source, drain, and bulk) is defined as:

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}, \qquad i \text{ or } j \in (g, d, s, b). \tag{5}$$

BSIM4 provides three options for selecting different capacitance models. By selecting different capMod options, different model equations can be used to describe the characteristics of the charge and the capacitances [5]. In this model, the source/drain series resistances are modeled by a bias-independent diffusion resistance and bias-dependent LDD resistances. Accurate modeling of the bias-dependent LDD resistances is important for deep submicron CMOS technologies. The LDD source/drain resistance $R_{ds}(V)$ is modeled internally through the I-V equation. The detailed relationships for modeling of intrinsic resistances have been given in [5]. Then the values of the per-unit-length intrinsic elements can be obtained by using scaling rules [6].

The extrinsic part models the transmission line and distributed behavior of transistor along the electrodes width. Therefore, the per-unit-length 3-by-3 square impedance and admittance matrices of transmission line MOSFET model, as a six-port structure, can be written as:

$$\begin{aligned}\left[\hat{Y}\right] &= \left[\hat{Y}_{extrinsic}\right] + \left[\hat{Y}_{intrinsic}\right] \\ &= \left[G\right] + j\omega\left[C\right] + \left[\hat{Y}_{tr}\right],\end{aligned} \tag{6}$$

$$\left[\hat{Z}\right] = \left[Z_s\right] + j\omega\left[L\right] = \left[R\right] + j\omega\left[L_i\right] + j\omega\left[L\right], \tag{7}$$

where [C], [G] and [L] are the per-unit-length matrices of capacitance, conductance and inductance, respectively. The entries in these matrices can be obtained by applying numerical methods of calculating the per-unit-length parameters for multi-conductor transmission lines [7], according to the electrical and physical characteristics of the transistor. Furthermore, $[Z_s]$ is the surface impedance matrix and demonstrates the distributed effects and frequency-dependent losses caused by the skin effect. The real part of $[Z_s]$ represents the electrode resistance and the imaginary part, the internal inductance [6]. $[Y_{tr}]$ is used to model the intrinsic parallel part of the distributed transistor model. By applying the transmission line theory to the transistor model of Fig. 1 (b), the second-order coupled equations in the frequency-domain can be written as:

$$\frac{d^2[\hat{V}]}{dz^2} = \frac{d^2}{dz^2}\left[\hat{V}_d \ \hat{V}_g \ \hat{V}_s\right]^T = -\left[\hat{Z}\right]\left[\hat{Y}\right]\left[\hat{V}\right], \tag{8}$$

$$\frac{d^2[\hat{I}]}{dz^2} = \frac{d^2}{dz^2}\left[\hat{I}_d \ \hat{I}_g \ \hat{I}_s\right]^T = -\left[\hat{Y}\right]\left[\hat{Z}\right]\left[\hat{I}\right], \tag{9}$$

where [V] and [I] are 1-by-3 voltage and current matrices of electrodes, respectively and functions of z and ω. For solving the above equations, the well-known similarity transformation solution is used [8]. By implementing this method, the general solutions for the voltages and current matrices can be obtained as:

$$\left[\hat{V}\right] = \left[\hat{T}_V\right]\left(\left[e^{-\hat{\gamma}z}\right][\hat{V}_m^+] + [e^{+\hat{\gamma}z}]\left[\hat{V}_m^-\right]\right), \tag{10}$$

$$\left[\hat{I}\right] = \left[\hat{Y}_c\right]\left[\hat{T}_V\right]\left(\left[e^{-\hat{\gamma}z}\right]\left[\hat{V}_m^+\right] - [e^{+\hat{\gamma}z}]\left[\hat{V}_m^-\right]\right), \tag{11}$$

where $[\hat{Y}_c] = [\hat{Z}]^{-1}[\hat{T}_V][\hat{\gamma}][\hat{T}_V]^{-1}$ is defined as characteristic admittance matrix. The elements of $[\hat{\gamma}]$ and $[\hat{T}_V]$ matrices are the eigenvalues and eigenvectors of $[\hat{Z}][\hat{Y}_c]$, respectively. By evaluating the general forms of the solutions in (10) and (11) at z = 0 and z = W and omitting the unknown coefficients $[\hat{V}_m^{\pm}]$, the 6-by-6 chain matrix of MOSFET model shown in Fig. 1 (b), which can be transformed to the scattering matrix form, will be obtained as follows:

$$\begin{aligned}\left[\hat{V},\hat{I}\right]^T_{(W,\omega)} &= -\hat{\Phi}\Big|_{(W)}\left[\hat{V},\hat{I}\right]^T_{(0,\omega)} \\ &= \begin{bmatrix}\hat{\Phi}_{11\ 3\times3} & \hat{\Phi}_{12\ 3\times3} \\ \hat{\Phi}_{21\ 3\times3} & \hat{\Phi}_{22\ 3\times3}\end{bmatrix}_{(W)}\left[\hat{V},\hat{I}\right]^T_{(0,\omega)},\end{aligned} \tag{12}$$

$$\begin{aligned}\hat{\Phi}_{11}\Big|_{(W)} &= \frac{1}{2}\hat{T}_V(e^{\hat{\gamma}W} + e^{-\hat{\gamma}W})\hat{T}_V^{-1}, \\ \hat{\Phi}_{12}\Big|_{(W)} &= -\frac{1}{2}\hat{T}_V(e^{\hat{\gamma}W} - e^{-\hat{\gamma}W})\hat{\gamma}^{-1}\hat{T}_V^{-1}\hat{Z}, \\ \hat{\Phi}_{21}\Big|_{(W)} &= -\frac{1}{2}\hat{Y}_c\left[\hat{T}_V\left(e^{\hat{\gamma}W} - e^{-\hat{\gamma}W}\right)\hat{T}_V^{-1}\right], \\ \hat{\Phi}_{22}\Big|_{(W)} &= \frac{1}{2}\hat{Z}^{-1}\hat{T}_V\left(e^{\hat{\gamma}W} + e^{-\hat{\gamma}W}\right)\hat{T}_V^{-1}\hat{Z}.\end{aligned} \tag{13}$$

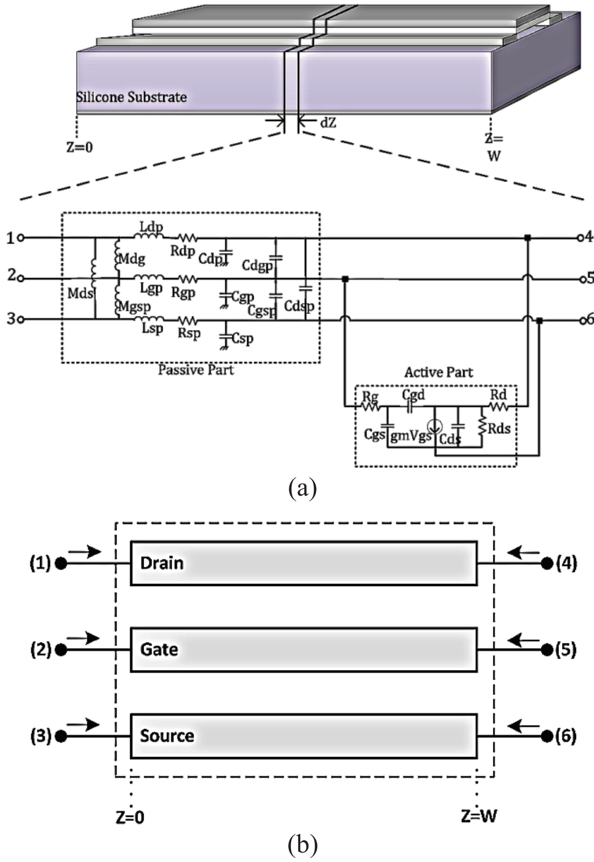

Fig. 1. (a) Differential part of distributed signal model of the mm-wave MOSFET, and (b) the six-port distributed transmission line model of MOSFET.

B. Distributed noise analysis of millimeter wave MOSFET

To consider the distributed electrodes width effect, the excited three-coupled transmission line structure, exciting by noise equivalent sources distributed on the conductors, is proposed for modeling of noise performance of millimeter wave MOSSFETs. A full description of the proposed model is clearly shown in Fig. 2. The noise originated within the active region is computed by using BSIM4 model [5]. It includes the flicker noise, channel thermal noise, induced gate noise and their correlation and thermal noise due to the resistances at the terminals. Two flicker noise models are included in BSIM4. In this paper, unified physical flicker noise model is used. In this model, the spectral drain current noise power density is formulated as:

$$\mathrm{S_{id}}(f)=\frac{\mathrm{S_{id,inv}}(f).\mathrm{S_{id,sub}}(f)}{\mathrm{S_{id,inv}}(f)+\mathrm{S_{id,sub}}(f)}\,, \tag{14}$$

where $\mathrm{S_{id,inv}}(f)$ and $\mathrm{S_{id,sub}}(f)$ are the spectral drain current noise power density of the device in the inversion and the sub-threshold regions, respectively, which the detailed equations of them have been given in [5]. Such as flicker noise, two options for the channel thermal noise are provided in BSIM4. One is the charge-based model from BSIM3v3 and the other is the holistic model. In the holistic model, which is used in this paper, all the short-channel effects including the velocity saturation effect incorporated in the I–V model as well as the induced gate noise with partial correlation to the channel thermal noise are all captured in the new "noise partition" model. In this model, two current and voltage noise source is used for modeling. The noise voltage source partitioned to the source side is given by:

$$\overline{v_d^2}=4k_B\mathrm{T}\theta_{tnoi}\frac{\mathrm{V_{dseff}}\,\Delta\mathrm{f}}{\mathrm{I_{DS}}}, \tag{15}$$

and the noise current source put in the channel region with gate and body amplication is given by:

$$\begin{aligned}\overline{i_d^2}=&\frac{4k_B\mathrm{TV_{dseff}}\Delta\mathrm{f}}{\mathrm{I_{DS}}}\left[G_{DS}+\beta_{tnoi}(G_m+G_{mbs})\right]^2\\&-\overline{v_d^2}\left(G_{DS}+G_m+G_{mbs}\right)^2.\end{aligned} \tag{16}$$

Finally, the power spectral density of the thermal noise current from the electrodes resistance is given by [5]:

$$S_{it,R_{g,d,s}}=\frac{4K_BT}{R_{g,d,s}}.\frac{1}{2}. \tag{17}$$

Aside from the intrinsic noise sources, the thermal noise generated within the passive part is considered. By considering the noise sources as excited sources, the transistor noise behavior can be analyzed by using excited multi conductor transmission lines solutions [9].

As shown in Fig. 2, all the noise sources of any differential subsections of the model can be transformed into correlated input-referred voltage and current noise sources of a noise free network, by using circuit analysis [10]. Then, by using Kirchhoff's voltage (KVL) and current (KCL) laws for the differential segment, the frequency domain coupled first-order ordinary differential equations of the noise transmission line model of the transistor will be obtained:

$$\frac{d}{dz}\begin{bmatrix}\hat{V}\\\hat{I}\end{bmatrix}_{(z,\omega)}=\begin{bmatrix}0&-\hat{Z}\\-\hat{Y}&0\end{bmatrix}\begin{bmatrix}\hat{V}\\\hat{I}\end{bmatrix}_{(z,\omega)}+\begin{bmatrix}\hat{v}_n\\\hat{i}_n\end{bmatrix}_{(z)}, \tag{18}$$

where $[\hat{\mathrm{v}}_\mathrm{n}]_{(z)}$ and $[\hat{\mathrm{i}}_\mathrm{n}]_{(z)}$ are 1-by-3 matrices of the linear density of voltage and current noise sources, respectively. Equation (18) is in the same form as state-variable equation, thus the solution of it can be written as [11]:

$$\begin{bmatrix}\hat{V}\\\hat{I}\end{bmatrix}_{(z,\omega)}=\hat{\Phi}\Big|_{(z-z_0)}\begin{bmatrix}\hat{V}\\\hat{I}\end{bmatrix}_{(z_0,\omega)}+\int_{z_0}^{z}\hat{\Phi}\Big|_{(z-\tau)}\begin{bmatrix}\hat{v}_n\\\hat{i}_n\end{bmatrix}_{(z)}d\tau. \tag{19}$$

By substituting $z_0 = 0$ and $z = W$, the effect of the internal noise sources on the voltage and current of the transistor port can be determined as follows:

$$\begin{bmatrix}\hat{V}\\ \hat{I}\end{bmatrix}_{(W,\omega)}=\begin{bmatrix}\hat{\Phi}_{11} & \hat{\Phi}_{12}\\ \hat{\Phi}_{21} & \hat{\Phi}_{22}\end{bmatrix}_{(W)}\begin{bmatrix}\hat{V}\\ \hat{I}\end{bmatrix}_{(0,\omega)}+\begin{bmatrix}\hat{V}_{NT}\\ \hat{I}_{NT}\end{bmatrix}_{(W)}, \quad (20)$$

where:

$$\begin{bmatrix}\hat{V}_{NT}\\ \hat{I}_{NT}\end{bmatrix}_{(W)}=\underbrace{\int_0^W\begin{bmatrix}\hat{\Phi}_{11} & \hat{\Phi}_{12}\\ \hat{\Phi}_{21} & \hat{\Phi}_{22}\end{bmatrix}_{(\tau)}d\tau}_{[\hat{A}(W)]_{6\times 6}}.\begin{bmatrix}\hat{v}_n\\ \hat{i}_n\end{bmatrix}. \quad (21)$$

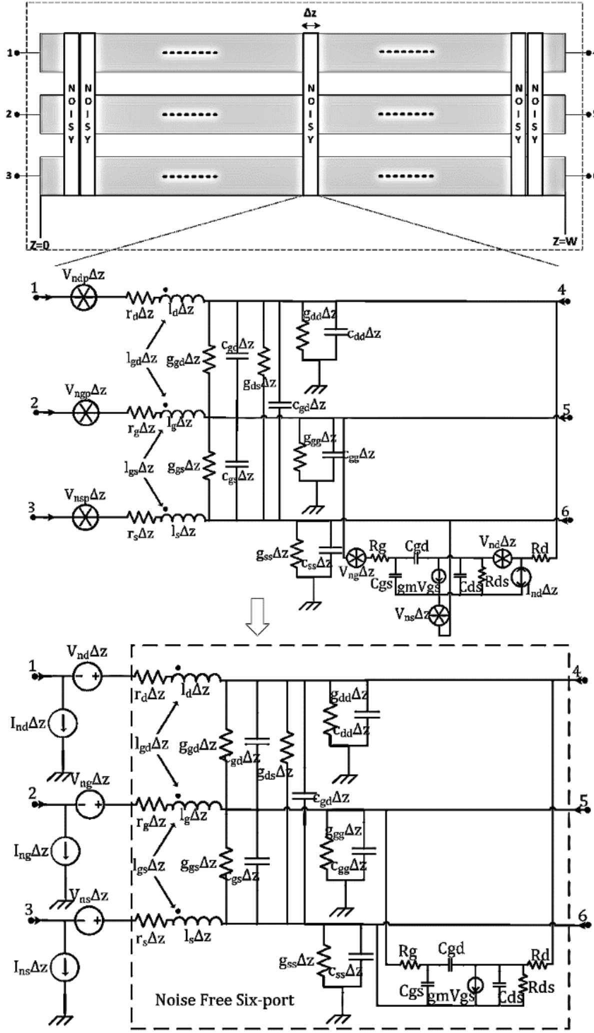

Fig. 2. Complete details of distributed noise model of the mm-wave MOSFET as excited three-coupled transmission line structure.

The distributed noise sources of differential part in (21) are assumed to be independent of the device width, since the BSIM4 model is chosen for them. The correlation matrix for admittance representation can be obtained by determination of the currents in short-circuited ports of transistor [12]. By enforcing boundary conditions to equation (20), the noise currents at the short-circuited ports, as a six-port active network, can be written in the following matrix form:

$$\begin{bmatrix}\hat{I}_{n0}\\ \hat{I}_{nW}\end{bmatrix}=\begin{bmatrix}-\hat{I}\big|_{(0,\omega)}\\ +\hat{I}\big|_{(W,\omega)}\end{bmatrix}=\underbrace{\begin{bmatrix}\hat{Z}^{-1} & \mathrm{K}\\ -\hat{Z}^{-1} & \mathrm{K}\end{bmatrix}}_{P}\times\begin{bmatrix}\hat{v}_n\\ \hat{i}_n\end{bmatrix}, \quad (22)$$

for $\mathrm{K}=-\hat{T}_I\hat{\gamma}^{-1}\sinh^{-1}(\hat{\gamma}W)(\cosh(\hat{\gamma}W)-1_{3\times3})\hat{T}_I^{-1}$. Finally, the correlation matrix for admittance representation of the six-port noise model of the MOSFET can be written as equation (23). CAU is the per-unit-length noise correlation matrix for chain representation of the transistor:

$$CY_{tr}=\begin{bmatrix}I_{n0}\\ I_{nW}\end{bmatrix}\begin{bmatrix}I_{n0}\\ I_{nW}\end{bmatrix}^{\dagger}=P\underbrace{\begin{bmatrix}\hat{v}_n\\ \hat{i}_n\end{bmatrix}\begin{bmatrix}\hat{v}_n\\ \hat{i}_n\end{bmatrix}^{\dagger}}_{CAU}P^{\dagger}. \quad (23)$$

III. RESULTS AND DISCUSSION

The proposed approach is used for modeling of a 130 nm bulk CMOS transistor. It is sufficient to consider introduced model for a single finger structure. Multiple fingers transistors can be accounted as parallel multiple single finger transistors. The transistor is biased at Vds = 1.2 V and Ids = 7 mA. As was mentioned in the previous section, the BSIM4 model [5], is used to compute elements and noise sources of active part and the per-unit-length parameters of passive part is evaluated by using numerical method of moments technique [7]. As shown in Fig. 1, the beginning of the gate and the end of drain electrodes are considered as the input and output nodes, respectively. Moreover, the source electrodes are grounded.

The scattering and noise parameters of proposed distributed model and Cadence SpectreRF post-layout simulation results are displayed in Figs. 3 and 4, for an NMOS transistor with gate width of 10 µm. The excellent broadband accuracy of the distributed model compared to the simulation results verifies that the introduced model is correct and complete. Furthermore, comparing these curves with lumped model, one can see that third models agreed well at low frequency but at high frequencies, the distributed effects of the transmission line capacitances and inductances along the device width become significant and can no longer be ignored. The scattering parameters of the transistor with gate width of 90 µm, over a frequency range of DC–100 GHz, calculated by using proposed distributed and lumped models are drawn in Fig. 5. The results clearly show that the distributed and lumped models are the same at the low frequency and by increasing the frequency, the difference between two models also increasing. The S11 and S21 of the transistor for three values of the gate width, 10, 60 and 90 µm, are plotted in Fig. 6.

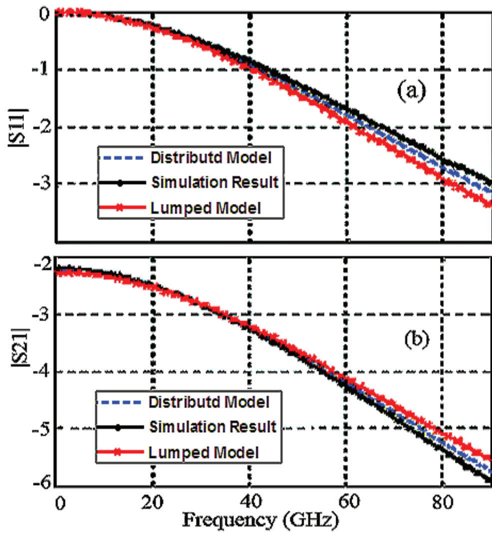

Fig. 3. Scattering parameters of 10 µm MOSFET.

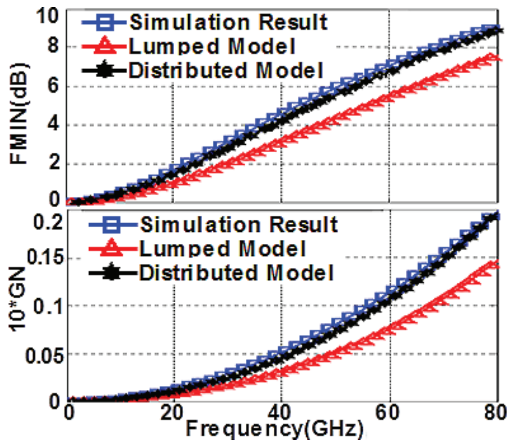

Fig. 4. Noise parameters of 10 µm MOSFET.

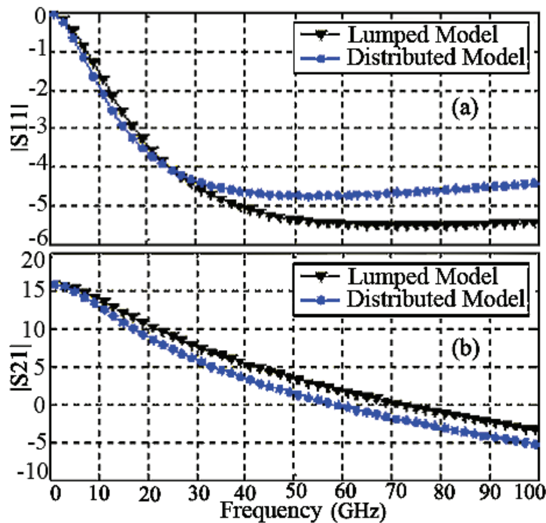

Fig. 5. Scattering parameters of 90 µm MOSFET.

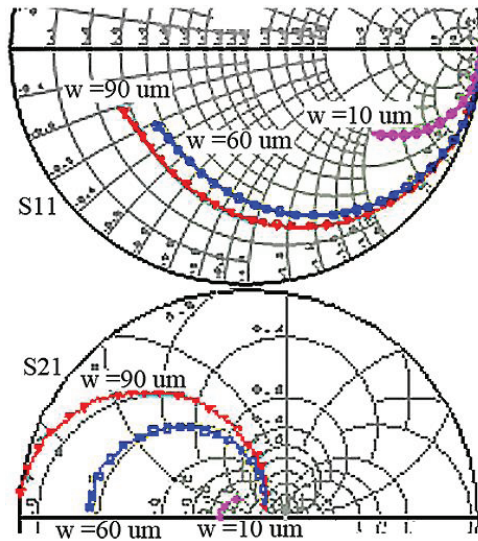

Fig. 6. Scattering parameters of 10, 60, and 90 µm MOSFETs computed by distributed model.

By using introduced model, four noise parameters, including minimum noise figure, normalized equivalent noise admittance, the amplitude and the phase of optimum reflection coefficient, are plotted in Fig. 7 and compared with lumped model. Moreover, Fig. 8 shows the behavior of minimum noise figure of the transistor for the different values of the gate width. Studying these figures illustrates the importance of distributed transmission line modeling of MOSFET by increasing the device width and the frequency.

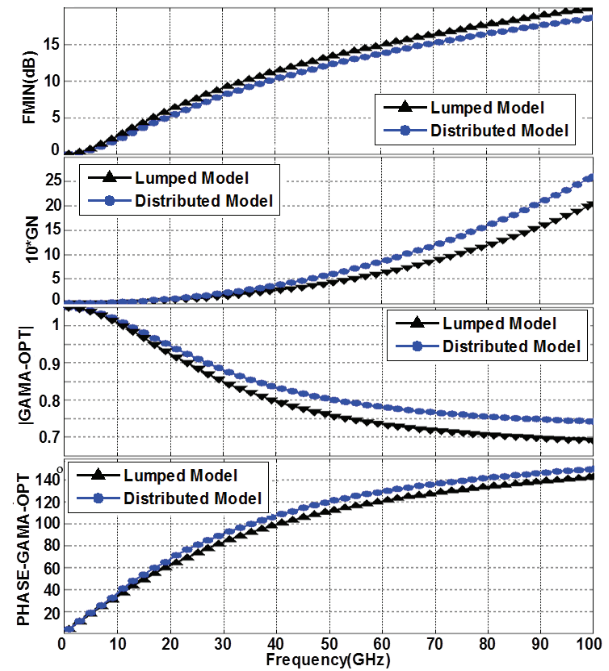

Fig. 7. Noise parameters of the MOSFET.

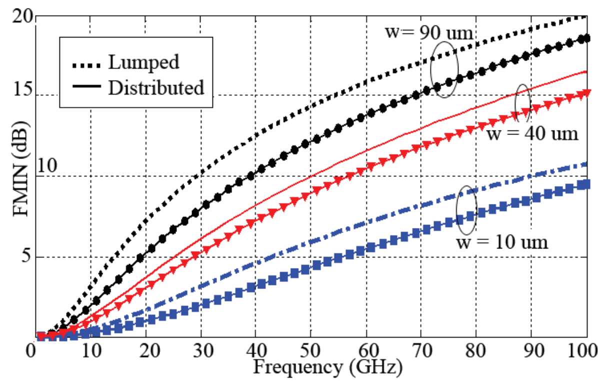

Fig. 8. Minimum noise figure of the MOSFET.

Figure 9 demonstrates the constant noise figure and available power gain circles of the MOSFET at 20 and 60 GHz. Thus, based on the information obtained from the proposed approach, accurate design of mm-wave circuits, containing the MOSFET, for a specified noise figure and available power gain is possible.

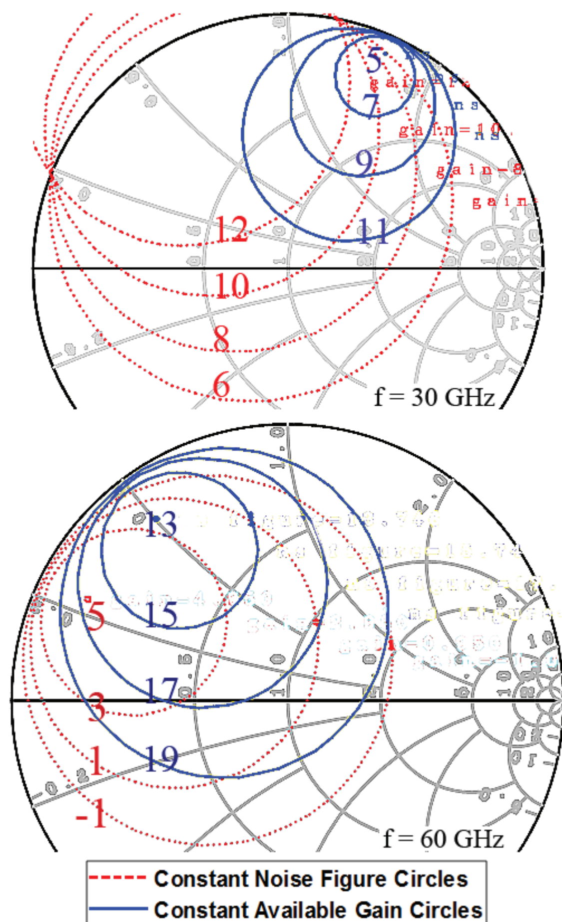

Fig. 9. Constant noise figure and available gain circles calculated by distributed model for f = 30 and 60 GHz.

IV. CONCLUSION

As the operating frequency of MOSFETs increases to the mm-wave range, the width of the device become comparable to the wave length. In such cases, the distributed transmission line effect needs to be considered accurately, in device modeling. According to that in the previous lumped models this effect wasn't considered, this paper introduces a new distributed transmission line signal and noise modeling and analysis of mm-wave MOSFET transistor. In this model, the MOSFET transistor is considered as the excited three-coupled active transmission line structure, exciting by noise equivalent sources distributed on its conductors. Comparing the signal and noise parameters of MOSFET calculated with the proposed distributed model and lumped model was shown that two models have the same results at low frequencies. But, by increasing frequency to the mm-wave range, where the electrodes widths are comparable with the wavelength, a difference appears between the results of two models. It is demonstrated that the distributed effects of the transmission line along the device width become significant and can no longer be ignored. Therefore, the accuracy of high-frequency noise simulation in the Nano-scale RF CMOS transistors can be facilitated by using the proposed model. Moreover, based on the proposed modeling approach, the influence of important factors such as the effect of electrode loading and the location and number of excitation/ extraction contact points, can be investigated and optimized for improving the performance of the mm-wave MOSFETs.

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