Preparation and Electrical Testing of Double Top Gate Graphene Field-Effect Transistor

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Abstract – In this paper, we prepare and test a graphene field-effect transistor with two top gates. The Fermi energy level of graphene can be adjusted by applying positive and negative voltages to the two top gates, and N-type and P-type graphene are formed in the channel region, thus inducing a graphene p-n junction. The current model is established using the gradual channel approximation (GCA) method, and the current and p-n junction characteristics of the device were obtained by formula simulations. Based on the principle of p-n junction luminescence, this device with graphene p-n junction is expected to achieve terahertz wave radiation with an appropriate optical resonant cavity.

Index Terms – current characteristics, GCA, graphene, p-n junction, terahertz.

I. INTRODUCTION

Graphene is a two-dimensional material with a hexagonal honeycomb-like planar lattice structure. As an emerging material, graphene is now used in a wide range of applications. For example, it can be used in electromagnetic devices such as various absorbers [1–3], due to its ability to change impedance by adjusting the bias voltage; It can be used in transistors [4–6] and antennas [7, 8] due to its excellent electrical and thermal properties; And most importantly, graphene materials are inextricably linked to terahertz science due to their unique band structure and linear dispersion relations. With carrier densities in the range of 10^9-10^{12} cm^{-2}, the plasma oscillation frequency of graphene materials lies in the terahertz band; Zero band gap graphene facilitates the generation of terahertz waves because the Fermi energy level in the p-n junction of graphene can be controlled by changing the gate to produce a smaller effective band gap encompassing the terahertz band. Terahertz has a lower wave frequency compared to the infrared and visible bands, and the terahertz conductance of graphene is stable when the frequency is changed, approximating the DC conductance over a wide range [9]; The bipolar electric field effect of graphene can be changed by applying an electric field to the Fermi energy level [10], and adjusting the Fermi energy level can also be achieved using light, magnetic fields, and chemical doping. Graphene has the above terahertz properties and is uniquely suited for research in the modulation, testing, and generation of terahertz waves.

Graphene FETs can be structurally classified into bottom-gate [11], top-gate [11–13], and double-gate type [14]. In conventional top-gate + back-gate p-n junction devices, the back gate is far from the graphene layer, challenging to regulate its Fermi energy level adequately. We designed a graphene field-effect transistor with 2 separated top gates in 2014 which was the first implementation at the time [15]. No one had made a device at the time, although others had proposed the double top gate

Submitted On: April 3, 2022
Accepted On: August 1, 2022

https://doi.org/10.13052/2022.ACES.J.370704

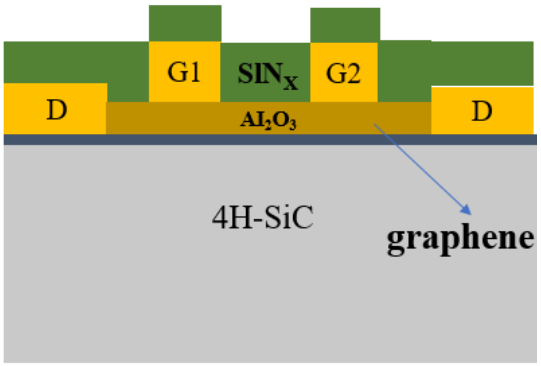


Fig. 1. Front view of DBR-DG-GFET.

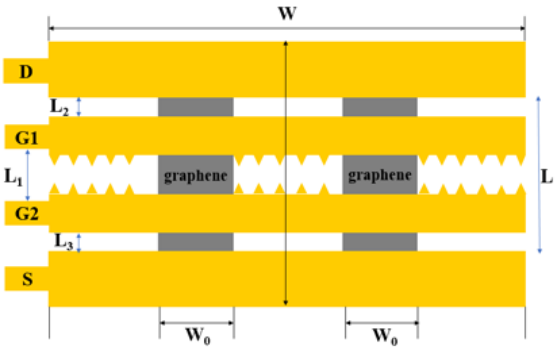


Fig. 2. Top view of DBR-DG-GFET.

structure. Its process does not require excessive energy injection while safeguarding the channel layer and improving stability. The current-voltage characteristics of the device are tested, and the results show that the gate voltage effectively induces the formation of a p-n junction in graphene, which is consistent with the theoretical analysis. Therefore, we will generate terahertz waves based on this gate-controlled p-n junction device in the future.

II. DESIGN AND WORKING PRINCIPLE

The front view of the device is shown in Fig. 1, graphene active region is between the dielectric layer AI_2O_3 and the substrate. The graphene substrate is 4H-SiC with a thickness of 500 μm, the source-drain, and two top-gate metal electrode uses Ti/Au (5/95 nm) alloy, the dielectric layer Al_2O_3 the waveguide SiNx (120 nm).

The top view of the device is shown in Fig. 2, graphene dimensions and the effect of graphene dimensions are as follows:

(1) Since only the zero-gap graphene can stably radiate terahertz photons, the graphene thickness must be 0.34 nm for a single layer.

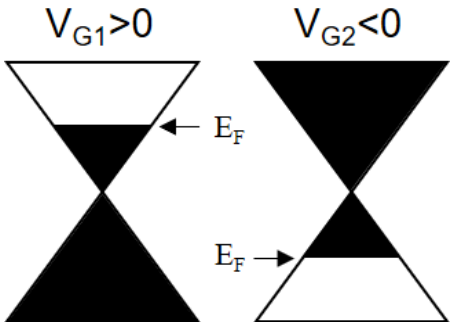


Fig. 3. Modulation of the Fermi energy level of graphene by a gate pressure.

(2) The total graphene length L is 260 μm, the distance between electrodes L_1= L_2 = 15 μm. The real impact on the output power is the length of the resonant cavity active region L_1. The smaller the gate gap L_0 the better but we set it to 30 μm due to the limitation of O_2 plasma etching.

(3) Graphene width W_0 is set as 100 μm. This value is influenced by the integration and fabrication process and is mainly determined by the design of the resonant cavity target

Figure 3 illustrates the Fermi energy level of graphene changes due to the gate voltage. With the positive gate voltage attracting electrons, the Fermi energy level moves upwards; The negative gate voltage attracts holes, so the Fermi energy level moves downwards, forming a p-n junction.

III. THEORETICAL CURRENT MODEL OF DG-GFET

Modeling the empirical channel current of the GFET helps us to analyze its electrical characteristic [16, 17]. Theoretical calculations are performed using GCA [17, 18] to clarify the operating mechanism of the DG-GFET under electrical injection.

With the source grounded, V_{G1} and V_{G2} are the gate voltages, and the forward bias voltage V_D is applied to the drain. Figure 4 shows a simplified device area containing only the insulating layer, metal gates, and channel, and the curve is the voltage drop along the channel. Both electrons and holes in DG-GFETs have the potential to become carriers due to the bipolar electric field effect of graphene, which is different from silicon-based transistors.

Where x is the length of a position in the channel area at x, the conductivity $\sigma(x,z) = n,p(x,z) \cdot e$. $n,p(x,z)$ is the number of electrons or holes per unit area. $Q = n,p \cdot e$ is the charge per unit area, L and W are the length and width of the channel, respectively. The carrier mobility defaults to a fixed value $\mu_{n,p}$, the conductance

at a point in the channel

$$g = \frac{\sigma(x,z)S(x,z)}{L} = \frac{W}{L}\int_0^{z_i}\sigma(z)\,dz$$
$$= \frac{W\mu_{n,p}}{L}\int_0^{z_i} e\cdot n,p(x,z)\,dz \quad (1)$$
$$= \frac{W\mu_{n,p}}{L}|Q(x)|,$$

where $Q(x) = -C_{ox}[V_G - V(x)]$ is the amount of charge stored per unit area at x, C_{ox} is the capacitance per unit area at the channel with $C_{ox} = \varepsilon\cdot\varepsilon_0/d$, ε and ε_0 is the insulation dielectric constant and vacuum dielectric constant, respectively. d is the insulation thickness, where V(x) is the bias voltage between x and the source. When dV the voltage varies on each dx, the microscopic expression for the drain current in the channel is

$$I_D = \mathrm{gL}\frac{dV}{dx} = \frac{W\mu_{n,p}|Q(x)|dV}{dx}$$
$$= \frac{W\mu_{n,p}}{L}C_{\mathrm{ox}}\frac{|V_G - V(X)|dV}{dx}, \quad (2)$$

then integrate from the source (x=0, V(x)=0) to the drain (x=L, V(x)=V_D) [19]

$$I_D = \frac{W\mu_{n,p}}{L}C_{\mathrm{ox}}\int_0^{V_D}|V_G - V(x)|\,dV. \quad (3)$$

As shown in Fig. 5 (a), if 0 < V_{G1}< V_D, V_{G2} = 0, the conducting carriers consist of two parts, the side near the source is electron accumulation, and from the source to the drain, the electron concentration gradually decreases to zero, and gradually turns to hole accumulation. Therefore, the drain current is superimposed by the drift of electrons (represented by black spheres) and holes (represented by white spheres) under the action of the drain voltage. Equation (4) is integrated by removing the absolute value and dividing it into two definition

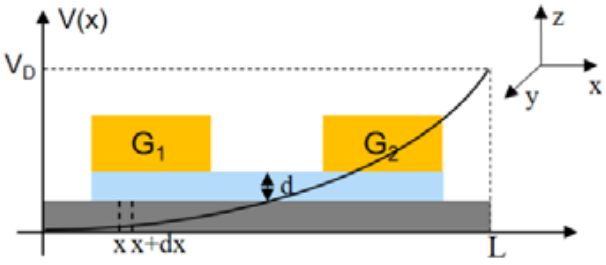


Fig. 4. Voltage distribution in the channel.

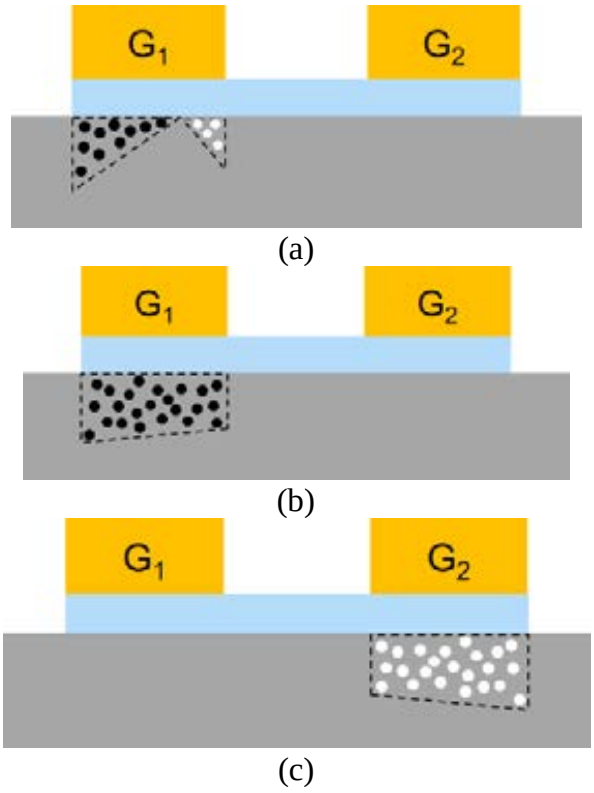


Fig. 5. Three carrier distributions for single gate applied pressure (a) 0<V_{G1}<V_D, V_{G2}=0 (b) V_{G1}>V_D, V_{G2}=0 (c) V_{G2}<0, V_{G1}=0.

domains:

$$I_D = \frac{W\mu_{n,p}}{L}C_{ox}\int_0^{V_D}|V_G - V(x)|\,dV$$
$$= \frac{WC_{ox}}{L}\left(\mu_n\int_0^{V_G}[V_G - V(x)]\,dV\right.$$
$$\left.+\mu_p\int_{V_G}^{V_D}[V(x) - V_G]\,dV\right) \quad (4)$$
$$= \frac{W}{2L}C_{ox}\left[\mu_n V_G^2 + \mu_p(V_G - V_D)^2\right].$$

In Fig. 5 (b), if the conditions $V_{G1} > V_D$ and V_{G2} = 0 are satisfied, the conducting carriers in the channel are mainly electrons, and the operating mechanism is primarily electron conduction when the voltage is applied at the drain. In Fig. 5 (c), if V_{G2}< 0, V_{G1} = 0, the conducting carriers in the channel are mainly holes, and the operating mechanism is primarily hole conduction:

$$I_D = \begin{cases} \frac{W}{2L}C_{ox}\left[\mu_n V_G^2 + \mu_p(V_G - V_D)^2\right] & 0 < V_{G1} < V_D, V_{G2} = 0 \\ \frac{W\mu_n}{L}C_{ox}\left(V_G V_D - \frac{V_D^2}{2}\right) & V_{G1} > V_D, V_{G2} = 0 \\ \frac{W\mu_p}{L}C_{ox}\left(\frac{V_D^2}{2} - V_G V_D\right) & V_{G2} < 0,\ V_{G1} = 0 \end{cases}. \quad (5)$$

As shown in Fig. 6 (a), when positive and negative voltages of the same magnitude are applied to the two

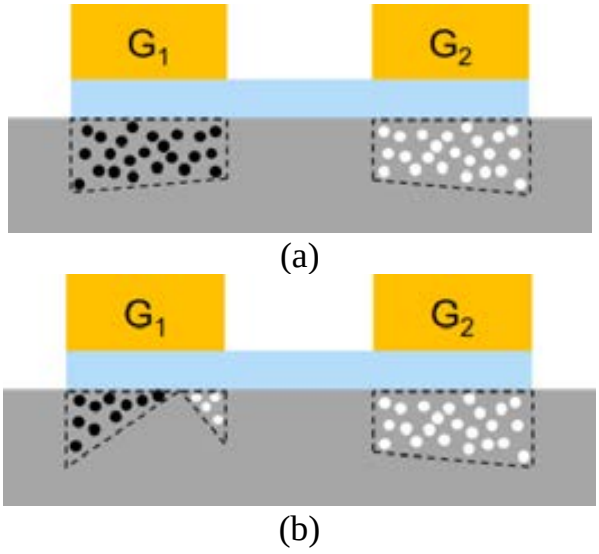


Fig. 6. Two carrier distributions for double gate applied pressure. (a) $V_G|>V_D$. (b) $0<|V_G|<V_D$.

top gates, and the absolute value of the gate voltage is greater than the drain voltage, electrons accumulate in the positive gate voltage region and holes accumulate in the negative gate voltage region. As shown in Fig. 6 (b), when positive and negative voltages of the same magnitude are applied to the two top gates, and the absolute value of the gate voltage is smaller than the drain voltage, electrons accumulate under the positive gate voltage region near the source. In contrast, holes accumulate under the positive gate voltage region near the drain and the negative gate voltage region. Referring to equation (4), the case is divided into two definition domains, and the integration is obtained as follows.

The channel resistance of each segment dR is

$$dR = \frac{dx}{gL} = \left(\frac{1}{W\mu_n |Q_n(x)|} + \frac{1}{W\mu_p |Q_p(x)|} \right) dx. \quad (6)$$

The formula for I_D is

$$I_D = \frac{gLdV}{dx} = \frac{W}{L} \int_0^{V_D} \left| \frac{\mu_n \mu_p |Q_n(x)| |Q_p(x)|}{\mu_p |Q_p(x)| + \mu_n |Q_n(x)|} \right| dV. \quad (7)$$

We get:

$$I_D = \begin{cases} t\frac{k}{1-k}\left(V_G V_D - \frac{V_D^2}{2}\right) & , \quad |V_G| > V_D \\ \frac{t}{2} \cdot \frac{k}{1-k}\left[V_G^2 + (V_G - V_D)^2\right], & 0 < |V_G| < V_D, \end{cases} \quad (8)$$

where $t = W\mu_n C_{0x}/L$, k $=\mu_p/\mu_n$.

The device parameters are set as follows: ε=9(the dielectric layer material is Al_2O_3), W=400 μm, L=60 μm, μ_n=10000 $cm^2/V \cdot s$, μ_p=4000 $cm^2/V \cdot s$, ε_0=8.85*10^{-14}F/cm, d=40 nm

$$t = \frac{W}{L}\mu_n \frac{\varepsilon_0 \varepsilon}{d} \approx 13.3 mA/V^2, k = \frac{\mu_p}{\mu_n} = 0.4. \quad (9)$$

By bringing t and k into equations (5) and (8), the operating current can be calculated for different gate voltage and bias voltage conditions, and the current characteristics of the device are plotted by Matlab.

Calculations explain the working mechanism of the device. Figure 7 (a) shows the output characteristic curve of the device under the single gate applied voltage. Positive gate voltage induces graphene to form an n-type semiconductor, and electrons accumulate in the channel area. When the drain-source bias voltage is small, electrons move toward the channel anode direction, creating a drift current, corresponding to the first linear region in the figure. As V_D gradually increases to a critical value, the drift of holes in the channel cannot be neglected. It moves in the opposite direction of electrons, preventing the increase of current, corresponding to the saturation

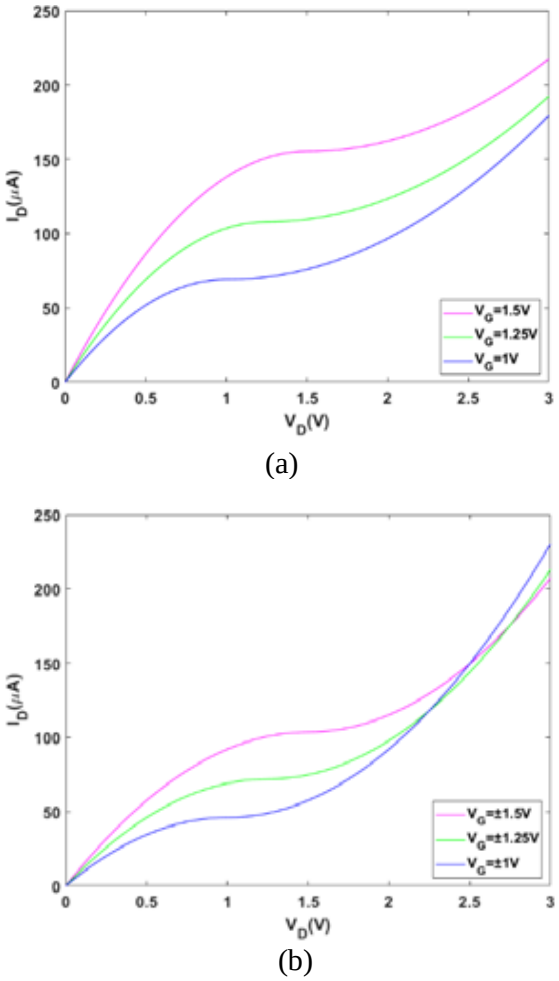


Fig. 7. I_D-V_D Output characteristic curve. (a) Single-gate applied voltage. (b) Double-gate applied voltage.

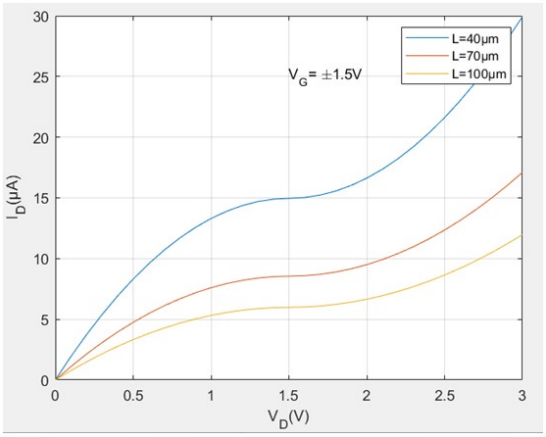
region in the figure. When V_D exceeds the critical value, the hole conductivity in the channel prevails, and the conductivity type of the channel changes from n-type to p-type, corresponding to the second linear region in the figure. Figure 7 (b) shows the output characteristic curve of the device under the double gate applied voltage, the positive gate pressure induces the accumulation of electrons in the graphene channel region, and the negative gate pressure induces the proliferation of holes in the graphene channel region, and the graphene p-n junction is formed in the channel region. When V_D is small, electrons move toward the positive pole, and holes move toward the negative. Because the electron mobility is much larger than the hole mobility, the channel still shows electron conduction. Still, the magnitude of the current is reduced compared to the single gate voltage, which reflects the weakening effect of the electric field built into the p-n junction on the drift current. Observe that a transient saturation region arises when the V_D gradually increases, and the conduction effects of electrons and holes are equivalent at this time; It is worth noting that when V_D increases to a certain level, a negative transconductance phenomenon occurs, indicating that the gate loses control of the current, which may be because a large gate voltage establishes a higher p-n junction barrier and suppresses the increase in output current.

According to equation (8), the parameters L and $k=\mu_p/\mu_n$ were also simulated to provide a reference for future improvements to the DG-GFET. Figure 8 (a) tells us that the channel length L should be reduced as much as the process can achieve. Figure 8 (b) illustrates that when considering graphene doping, increasing the k value helps to improve the performance of the device

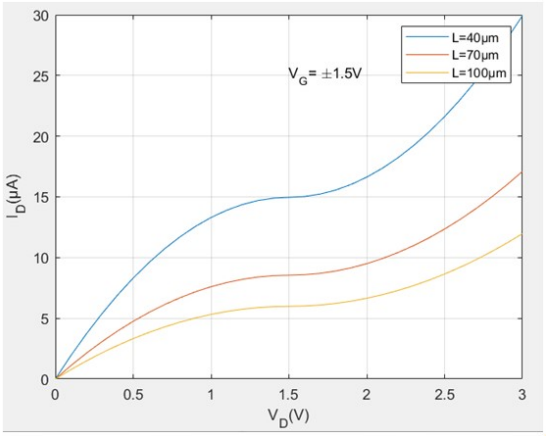
IV. DEVICE FABRICATION AND TESTING OF DEVICE

The device is observed under a 30 times microscope, as shown in, as shown in Fig. 9, and four gold wires are connected to the device's drain, source, and gate pins. The overall fabrication flow of the device is shown in Fig. 10, here are the details [20, 21]:

(1) Obtain monolayer graphene by thermal decomposition of 4H-SiC under low pressure and high-temperature environment using the epitaxial growth method.
(2) Cutting off the excess part of graphene, leaving only the graphene layer in the target region.
(3) Fabrication of leaky and source metal electrodes with Ti/Au material, mainly with process steps of gluing, exposure, development, metal deposition, and exfoliation.



(a)



(b)

Fig. 8. I_D-V_D Double gate output characteristic curve under, (a) different channel lengths L, and (b) different k.

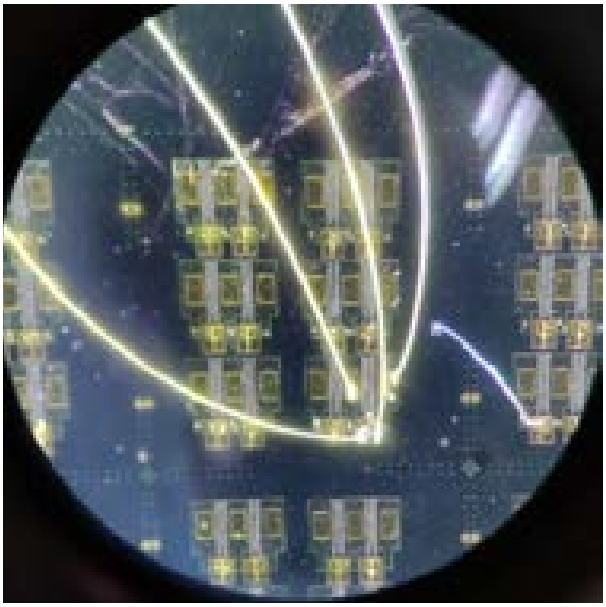


Fig. 9. Physical view of the device under a 30× microscope.

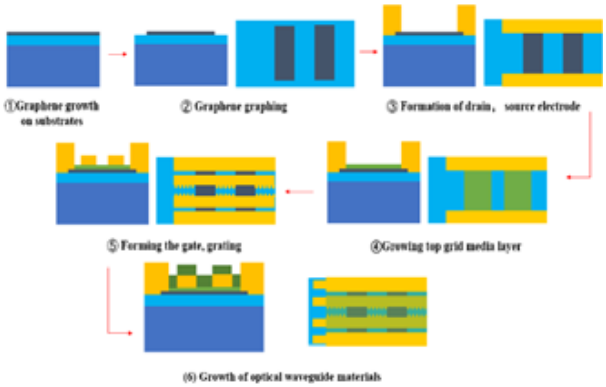


Fig. 10. DBR-DG-GFET fabrication steps.

(4) Deposition of Al_2O_3 media on graphene by atomic layer deposition (ALD), the ALD process allows precise control of the deposition thickness and high quality with fewer impurities.

(5) Growing two top gates with the same Ti/Au material, same steps as (3), it should be noted that the grating is attached to the gate and the size is small, requiring high precision, so a high level of the fabrication process is required.

(6) Deposition of waveguide material SiNx using plasma-enhanced chemical vapor deposition (PECVD) as the cavity material of the resonant cavity and coating on the device output port to improve the device output efficiency.

The potential difference between the gate and graphene determines the density of the two carriers in the device channel and whether the conducting type is electrons or holes. A sizeable forward gate voltage leads to the accumulation of electrons in graphene to produce an n-type channel. A sizeable reverse gate voltage leads to the accumulation of holes in graphene to build a p-type channel. This feature forms two branches separated by a Dirac point. After fabrication, electrical tests were performed on the double-top gate GFET. To obtain its transfer characteristic curve, the gate voltage V_{G1}= -3V-3 V, V_{G2}=0 V, and the drain-source V_D were 0.1 V and 0.2 V, respectively, to get its transfer characteristic curve, as shown in Fig. 11. The Dirac point of the intrinsic graphene is located at 0 V, and a bipolar curve shifted to the right is obtained because the substrate is heavily doped silicon, and the Dirac point is situated near 1.8 V, indicating that the graphene channel is P-type doped.

To eliminate the effect of graphene P-type doping, the value of the applied positive gate voltage needs to be greater than the Dirac point so that N-type graphene can be induced below this gate, thus forming a p-n junction. The output characteristics are tested by applying an appropriate forward drain voltage. Let V_{G2} be 1 V and V_{G1} be 3 V, 4 V, 5 V, and 6 V, and try the output characteristic curve of the device at the drain-source voltage V_D from 0 to 5 V Results are shown in Fig. 12.

Based on the results, when no gate voltage is applied, i.e., V_{G1}=V_{G2}=0 V, the graphene in the channel region is a good conductor, and the V-I curve is linear, as shown by the dashed line in Fig. 12. If there is no drain voltage, i.e., V_D=0, the p-n junction is in equilibrium, the current is zero, and the balance is broken after the drain bias is applied; When V_D gradually increases to the critical point of the p-n junction barrier, the growth trend of current turns; When V_D exceeds the breakdown point of the p-n junction barrier, the current increases significantly and enters into another linear growth region. It is worth mentioning that when V_D increases to a certain degree a negative transconductance phenomenon appears, which is due to the large gate voltage establishing a higher p-n junction barrier, resulting in a lag in the growth turning point of output current. Overall, the experimental results demonstrate that applying an external bias voltage to the double-top gate device effectively induces graphene to form a p-n junction.

V. RESULTS AND DISCUSSION

This paper designs and fabricates a graphene p-n junction device with a double-top gate structure. Comparing experimental test data versus simulation results, the default channel in simulation is pure graphene. The Dirac point is located at 0 V The gate voltage injection is positive and negative with equivalent absolute values. The actual device has a Dirac point shift in the graphene leading to a difference in the gate voltage setting. The measured data are consistent with the simu-

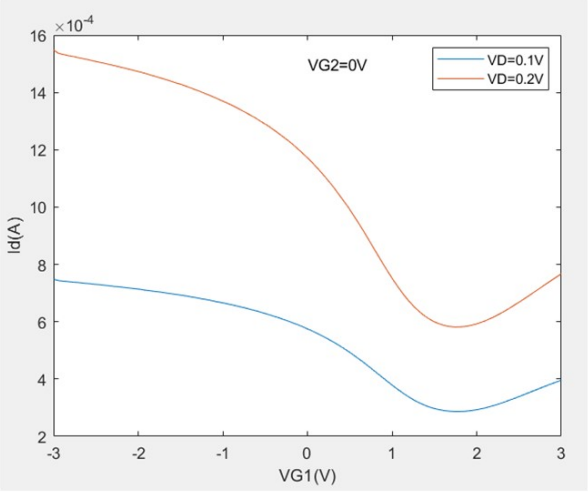


Fig. 11. Transfer characteristic test curve.

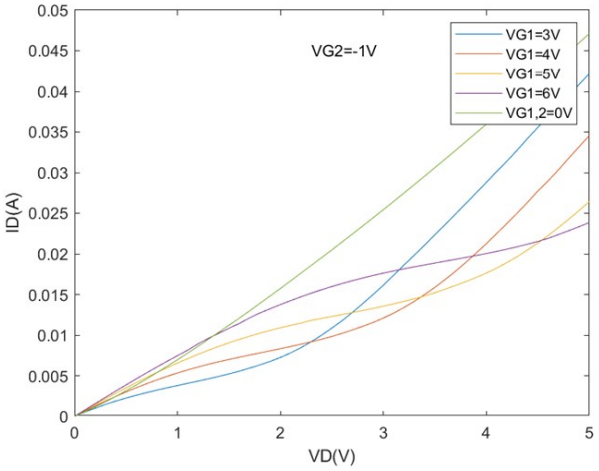


Fig. 12. Output characteristics test curve.

lation results. When the injected bias voltage is small, larger the gate voltage causes the graphene channel to accumulate more non-equilibrium carriers, at which time the current operating increases linearly with the rise of the gate voltage; when the bias voltage is raised to the critical point of breaking through the p-n junction barrier, the trend of current growth turns; When the bias voltage reaches the p-n junction barrier-breaking point, the current starts to increase significantly and enters into the faster linear growth region. A large gate voltage will increase the barrier height of the p-n junction to a certain extent, and the negative transconductance phenomenon appears, which suppresses the continuous increase of the current. Since simulation parameters are less accurate than in perfect theoretical conditions, there are some numerical errors, but overall the model is quite reliable.

ACKNOWLEDGMENT

This work is supported by National Natural Science Fund (61871442), Ministries Fund (6142601200504, 2020-JCJQ-JJ-3 97) funding.

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