

A Compact Four-way Quadrature Power Splitter for 5G Low-band Applications

Song Gao¹, Hao Wang¹, Kwok L. Chung^{2,*}, Yingsong Li³, Kangtai Zheng², and Luqi Chen²

¹Civionics Research Laboratory, School of Civil Engineering
Qingdao University of Technology, Qingdao, 266000, China
gaosong@qut.edu.cn, hason1997@163.com

²School of Computer Science and Engineering
Huizhou University, Huizhou, 516007, China
*klchung@hzu.edu.cn, 2014080902233@stu.hzu.edu.cn, 2014080902429@stu.hzu.edu.cn

³Key Laboratory of Intelligent Computing and Signal Processing
Ministry of Education, Anhui University, China
liyingsong@ieee.org

Abstract – This article introduces an ultra-compact four-way quadrature power splitter (4W-QPS) based on a novel transmission-line compression technique called double-path zigzag microstrip line (DP-ZML). Detailed design techniques with modular approach are disclosed for the state-of-the-art 5G low-band applications. The theoretical predictions are verified with experimental results through a fabricated prototype that operates from 696.55 to 876.03 MHz with >15 dB return-losses and isolations, and $90^\circ \pm 4^\circ$ quadrature phase between adjacent outputs. The compact size of this 4W-QPS is achieved at $0.21\lambda_g \times 0.21\lambda_g$ at a center frequency of 786 MHz.

Index Terms – 5G low-band, miniaturization, quadrature power splitter (QPS), Z-shaped microstrip line.

I. INTRODUCTION

According to 3GPP TS38.101-1 V15.3.0 [1], New Radio Frequency Ranges (NR-FRs) are being rolled out into fifth generation (5G) mobile communications, where power dividers/splitters play a vital role in 5G low frequency bands. The 5G low-band spectrum is classified as any spectrum that operates below 1 GHz, e.g., 700~800 MHz, like n12, n14, n18, and n20 [1]. A four-way quadrature power splitter (4W-QPS) with constant phase-shifts is in high demand by circularly-polarized antennas, multiple-beam antennas and power amplifiers due to its simplicity and low power loss. On one hand, conventional power dividers are known to occupy a large physical size due to restriction of multiple quarter-wavelength ($\lambda/4$) transmission lines. On the other hand, a large foot-print is required for the QPSs operating

in the 5G low-band NR at frequencies of 800 MHz or so.

Over the years, many miniaturization techniques of power splitter circuits and or feeding networks using various types of transmission lines have been reported in the literature [2–5]. In [4–5], broadband QPSs using metamaterial lines were proposed for circularly-polarized antenna array, wherein the quadrature (90°) phase difference between output ports was realized by space-saving metamaterial lines. Based on half-wavelength slot-lines coupling, a compact four-way out-of-phase power splitter was proposed in [6]. However, the isolations between output ports are identified to be insufficient (<15 dB), which may not be suitable for certain applications that require high isolations. To address this issue, a new radial power divider was reported in [7], wherein an isolation network composed of RLC and LC topologies was used. Very good isolation levels (>20 dB) and its associated bandwidth were obtained; however, the air bridges used will increase fabrication cost as its footprint is big ($80 \times 80 \text{ mm}^2$) at 1 GHz. In [8], a four-way microstrip power splitter using lumped elements was proposed for dual-band (1 and 2 GHz) application. However, its electrical size ($0.54\lambda_g \times 0.45\lambda_g$) is found to be large. Recently, an interesting chained slotted power divider using half-mode substrate-integrated waveguide at X-band was presented [9], where compact size can be achieved at the cost of low isolation levels of about 12 dB. More recently, a very compact ($0.17\lambda_g \times 0.22\lambda_g$) quasi-planar four-way power splitter was reported [10], wherein high isolation (20 dB) bandwidth of 58% was achieved but with equal phases at its output ports. Similarly, a wideband (60%) equal-phase power

splitter (EPS) using multi-stage connection lines was reported in [11]. However, both the extra loss and broad size are found to be large.

In this paper, a highly compact four-way power splitter with quadrature phases using double-path Z-shaped microstrip line (DP-ZML) in the form of a double layer is presented. The goal of this compact design is to enable 5G low-band operation at a low cost. The predicted results are validated by a fabricated prototype presenting an operating bandwidth from 696.55 to 876.03 MHz, where its return losses and isolation are of >15 dB with phase-difference of $90^\circ \pm 4^\circ$ between adjacent output ports. The ultra-compact size is achieved at $0.21\lambda_g \times 0.21\lambda_g$.

II. GEOMETRY OF POWER SPLITTER USING DOUBLE-PATH ZIGZAG MICROSTRIP LINES

The initial geometry of the proposed double-path zigzag microstrip line in the form of four sections of ZML is shown in Fig. 1, which mimics a phase delay of 90° as in the single straight ML case (Fig. 1 (a)). The DP-ZML makes full use of PCB area and a common ground plane, wherein the ZMLs (zigzag traces) are positioned anti-symmetrically at the top- and bottom-side of the dual-layer FR4 substrate and electrically connected through three copper vias as shown in Figs. 1 (b) and 1 (c). In this way, the required length (phase delay) can be generated with an extremely small footprint on the circuit board. Meanwhile, owing to the short lines of

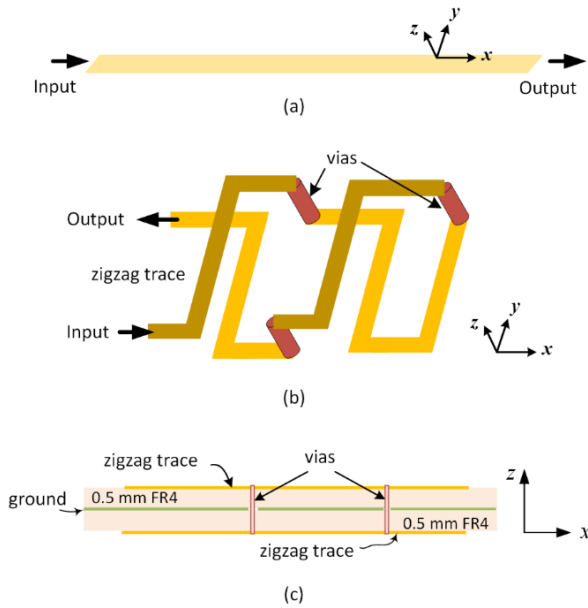


Fig. 1. Geometry of (a) conventional single straight ML, (b) proposed DP-ZML (substrates not shown), and (c) sideview of DP-ZMLs.

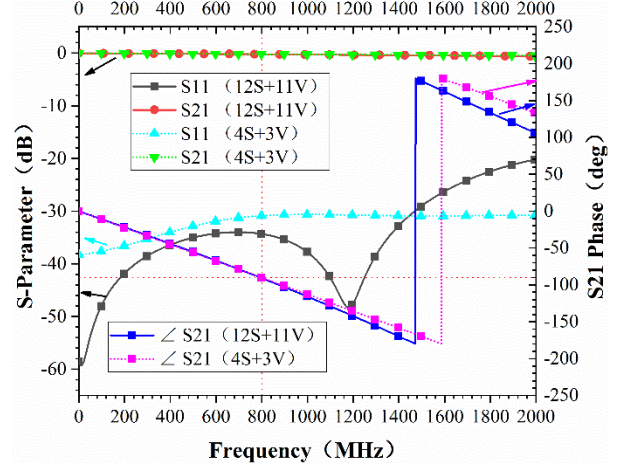


Fig. 2. Performance of zigzag MLs with 4 section and 12 section forms.

DP-ZML that owns a silent feature in reduction of coupling between microstrip lines printed on the same plane in comparison with parallel microstrip lines and or meander lines.

Figure 2 shows and compares the simulated performance of a four-section-plus-three-via (4S+3V) ZML design and a twelve-section-with-eleven-via (12S+11V) ZML design. The computed results are obtained by using a High Frequency Structure Simulator (HFSS) [12] in the frequency range of 0-2000 MHz. As seen, both the input and output reflection coefficients (S11 and S22) are tuned below -30 dB within the frequency range, whereas the neglectable insertion loss (S21) has been obtained, though a number of vias and zigzag sections have been used. These show that the internal impedance matching between the DP-ZML sections are well matched, whereas the tight schematic of the ZML shown perfect features low loss. More importantly, a quadrature phase delay at 800 MHz was obtained in both cases, and the phase delays varied linearly with frequency, viz., in the same manner with the single microstrip line.

III. QPS DESIGN METHODOLOGY AND LOGIC OPERATION

A stepwise design approach is employed to build the 4W-QPS as illustrated in Fig. 3, wherein four essential steps are described as follows:

- Step (a): design of $50\text{-}\Omega$ and $70.7\text{-}\Omega$ lines with different line widths.
- Step (b): design of 90° and 180° phase-delay ($50\text{-}\Omega$) lines with optimized number of metallic vias.
- Step (c): modular design of 2-way Wilkinson power splitter (2W-PS).
- Step (d): combination of PD lines with 2W-PSs by directly appending the PD lines to the outputs of PSs.

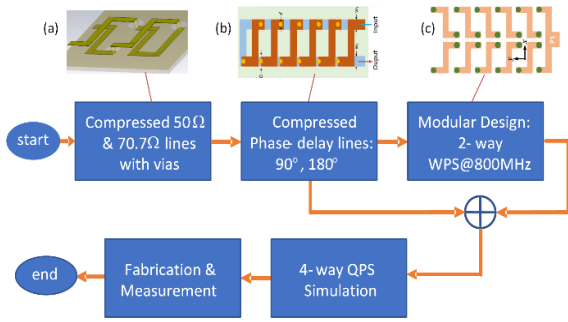


Fig. 3. Design logic-flow of 4-way QPS at 800 MHz.

After that, overall footprint optimization of 4W-QPS was undertaken using HFSS simulation, which composed of three building blocks of 2W-PS connected with three phase shifters, namely, two 90°- and one 180°-phase delays (PDs) in order to fulfill the requirement of 4W-QPS.

The geometry in the front- and back-view of the 2W-PS center at 800 MHz is shown in Fig. 4 (a), whereas its simulated performance is shown in Fig. 4 (b). As can

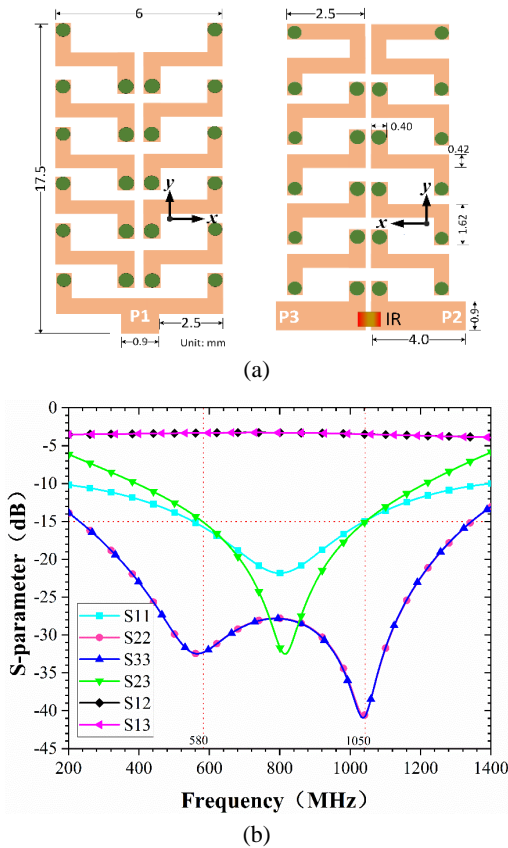


Fig. 4. Design of 2-way PS using DP-ZML at 800 MHz: (a) geometry, and (b) S-parameters performance.

be seen, the overlapped fractional bandwidth (FBW) was achieved from 580 to 1050 MHz (57.7%), wherein its return losses (-S11 and -S22) and isolation (-S23) were obtained higher than 15 dB, whereas the in-band insertion losses (-S21 and -S31) were about 3.4 dB. Viz., an extra loss of 0.4 dB was produced when 23 ZML sections and 22 vias were used.

IV. EXPERIMENTAL VERIFICATION AND COMPARISON

In order to verify the performance of the previously discussed design approach, a prototype of 4W-QPS was fabricated by employing DP-ZMLs printed on a 0.5mm-thick FR4 substrate ($\epsilon_r = 4.4, \tan\delta = 0.02$), as shown in Fig. 5. The photo illustrates the layout of the proposed QPS, including three blocks of 2W-PS, two 90°-PD and one 180°-PD. As shown, the footprint of the 4W-QPS prototype is compressed into a size of 45 mm × 45 mm ($0.21\lambda_g \times 0.21\lambda_g$ at 786 MHz, measurement) including the SMA output connectors. Each PS is optimized to operate at a stable bandwidth while maintaining a 3-dB coupling level, whereas the PDs are used to achieve constant phase difference in specific frequency bands. Meanwhile, the isolation of the circuit configuration is enhanced by three isolation resistors (IR) of 100-Ω. Therefore, it can be clearly seen that this 4W-QPS has a very simple and compact scale to be accommodated in integrated systems that cannot accommodate the area required for long transmission lines.

The predicted results were obtained by using HFSS in the frequency range of 300-1200 MHz whereas the measurement was undertaken by a network analyzer Agilent E8363C. Both the simulated and measured results are displayed and compared in Fig. 6. In general, there is a good agreement between the simulation and the measurement. The corresponding scatter-parameter

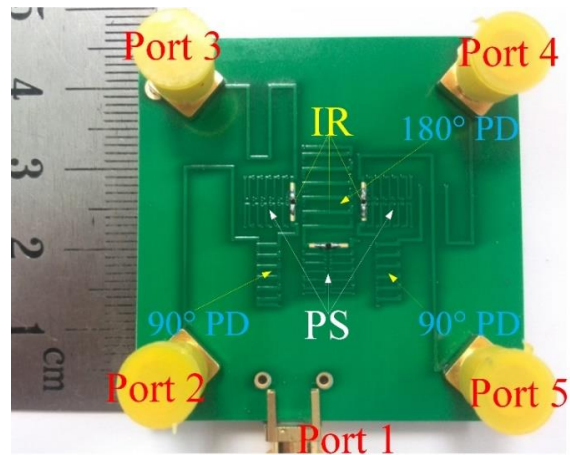


Fig. 5. Photograph of the fabricated 4-way QPS.

Table 1: Size and performance comparison of various four-way power splitters

Ref.	f_c (GHz)	4W-PSdesign	ϵ_r	Board size ($\lambda_g \times \lambda_g$)	Max EIL (dB)	15-dB FBW (%)	Iso ⁿ . at f_c (dB)
[4]	7.5	OPS	2.95	0.77×1.36	1.2	failed	17
[5]	1.0	EPS	4.5	0.52×0.52	2.0	24.4	25
[6]	1 & 2	EPS	3.66	0.54×0.45	0.2	42 & 14	24
[7]	9.3	EPS	3.5	2.21×0.27	1.5	failed	12
[8]	2.1	EPS	3.5	0.22×0.17	0.23	26.1	27
[9]	1.0	EPS	4.5	0.63×0.35	3.2	~60	32
This work	0.786	QPS	4.4	0.21×0.21	1.7	57.7	30

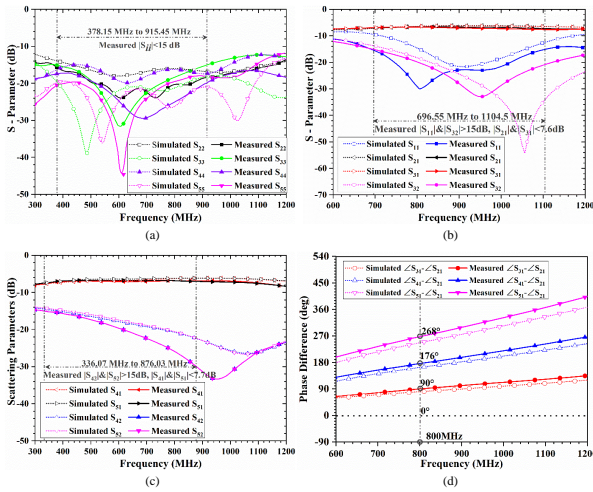


Fig. 6. Simulated and measured performance of the proposed 4W-QPS. (a) Output reflection coefficients (S22, S33, S44 and S55), (b) input reflection coefficient (S11), insertion losses (S21, S31), and isolation ($|S32|$), (c) insertion losses (S41, S51) and isolations (S42, S52), (d) output phase delays with respect to port-2.

magnitudes were recorded when exciting at the input (Port 1) with four outputs Port 2 to Port 5 (Fig. 5). An overlapped fractional bandwidth (FBW) is defined from 696.55 to 876.03 MHz, where the input and output return losses (viz., -S11, -S22, -S33, -S44, -S55) and isolations between output ports (viz., -S32, -S42, -S52) are all obtained better than 15 dB, as shown in Figs. 6 (a) to 6 (c). Moreover, the insertion losses among input and output less than 7.7 dB (maximum). Meanwhile, Fig. 6 (d) shows that the three output Ports (3, 4, and 5) of the 4W-QPS accomplish the phase difference of 0, 90°, 176°, 268° at 800 MHz (corresponding ideal values are 0, 90°, 180°, 270°) with respect to Port 2. These values imply a maximum phase error of 4° and a quadrature phase difference between adjacent outputs. Owing to the novel miniaturizing technique of DP-ZML, the footprint of the 4W-QPS circuit can realize a dramatic size reduc-

tion to 45 mm \times 45 mm at a center frequency of 786 MHz from measurement.

Since 4-way quadrature power splitters/combiners are in high demand in RF/microwave circularly-polarized antenna arrays, but designs of 4W-QPS are hardly available from the literature, Table 1 shows the size and performance of 4-way power splitters with different output phases. Most of them are equal-phase power splitters (EPSs) and one is for a 180° out of phase power splitter (OPS). In our design, the phase delays were implemented outside the PSs using DP-ZMLs, nonetheless, with the smallest electrical size ($0.21\lambda_g \times 0.21\lambda_g$) in the Table. Meanwhile, two of the listed designs failed to commit the common 15-dB overlapping fractional bandwidth (FBW) with low levels of port isolation at center frequencies. Our design committed 57.7% FBW with an isolation of 30 dB. Moreover, the maximum extra insertion loss (Max EIL) was achieved at 1.7 dB within the measured FBW, which is an acceptable level in the comparison.

V. CONCLUSION

An ultra-compact four-way quadrature power splitter using novel DP-ZML technique is presented in this paper. Unlike broadband 4W-QPSs that typically have no specific application for 5G low-band in the literature, the design objective here is a small footprint for dedicated applications at 5G low-band NR frequencies. As considered, the devised power splitter strikes a balance between remarkable transmission characteristics, phase deviation and minimum losses. Thanks to novel compression techniques, the overall circuit size is greatly reduced (45 mm \times 45 mm) compared to conventional planar microstrip lines for an operating bandwidth of 697 to 876 MHz with a maximum quadrature phase error of 4°, which is sufficient to cover 5G low-band NR n12, n14 and n20. This experiment shows that this novel two-layer Z-shaped microstrip line structure can also be applied to other passive components for miniaturization at low cost.

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Song Gao received his M.E. degree from the University of Stellenbosch South Africa in 2005 and his Ph.D. degree from Qingdao University of Technology (QUT) in 2013. He is now a full professor at the School of Civil Engineering, QUT, where he is also the head of the engineering materials laboratory. His main research interests are civionics transducers, high performance fiber reinforced cementation composites and high-performance building materials using recycled building waste.



Hao Wang was born in December 1997, Weifang, China. He received his Bachelor's degree from Qingdao Agricultural University in 2020. He is currently pursuing a Master's degree at QUT. His research interests include concrete structures and antenna-based sensors for structural health monitoring. In 2021, he participated in the IEEE ICEICT conference and received the "Best Paper Award". In 2022, he won second place in QUT's comprehensive scholarship prize.



Kwok L. Chung (Senior Member, IEEE) was a Research Professor and a supervisor of Ph.D. students at Qingdao University of Technology (QUT) from Dec. 2005 to Jan. 2021. He was the Director of Civionics Research Laboratory at QUT, where he led a cross-disciplinary research team for structural health monitoring. In April 2021, he joined Huizhou University as a Distinguished Professor. He has authored and coauthored about 180 publications [science citation index (SCI) and engineering index (EI)] in various areas of electrical and civil engineering. His current research interests include passive wireless sensors, cement-based materials design and characterization, clothing antennas, and intelligent reconfigurable surfaces.

Prof. Chung has been classified as one of the world's top 2% scientists in the 2020 and 2021 lists released by Stanford University. He is the Founding Chair of the IEEE Qingdao AP/MTT/COM joint chapter (CN10879) Beijing Section. He has been an Associate Editor of *IEEE Access* and an Associate Editor of Elsevier's

Alexandria Engineering Journal since 2016 and 2020, respectively. He is an active reviewer for numerous international journals from IEEE, Elsevier, IOPscience, and many others.



Yingsong Li received his B.S. degree in Electrical and Information Engineering, and M.S. degree in Electromagnetic Field and Microwave Technology from Harbin Engineering University, 2006 and 2011, respectively. He received his Ph.D. degree from both Kochi University of Technology (KUT), Japan and Harbin Engineering University (HEU), China in 2014. He is currently a full professor at the School of Electronic and Information Engineering at Anhui University since March 2022. He was a full professor in HEU from 2014 to 2022 and a visiting scholar at the University of California, Davis, from March 2016 to March 2017, a visiting professor at the University of York, UK in 2018, a visiting professor at the Far Eastern Federal University (FEFU) and KUT. Since 2018 he has held a visiting professorship at the School of Information of KUT from 2018. He is a Fellow of the Applied Computational Electromagnetics Society, and is also a senior member of the Chinese Institute of Electronics (CIE) and IEEE. He has authored and coauthored about 300 journal and conference papers in various areas of electrical and information engineering. His current research interests include signal processing, adaptive filters, metasurface designs and microwave antennas.

Dr. Li served as an Area Editor of *AEÜ-International Journal of Electronics and Communications* from 2017 to 2020. He is an Associate Editor of *IEEE Access*, *Applied Computational Electromagnetics Society (ACES) Journal*, the *Alexandria Engineering Journal* and *Electromagnetic Science*.

He was the TPC Co-Chair of the 2019 IEEE International Workshop on Electromagnetics (iWEM 2019-2020), 2019 IEEE 2nd International Conference on Electronic Information and Communication Technology (ICEICT 2019), 2019 International Applied Computational Electromagnetics Society (ACES) Symposium-China, 2019 Cross Strait Quad-regional Radio Science and the Wireless Technology Conference (2019 CSQRWC). He acts as a reviewer of numerous IEEE, IET, Elsevier and other international journals and conferences.



Kangtai Zheng (Student Member, IEEE) was born in April 2001, Guangdong, China. He is currently studying for a Bachelor's degree at the School of Computer Science and Computer Engineering at Huizhou University. His research interests include microwave antennas and components, intelligent reconfigurable surfaces and deep learning. In 2022, he participated in the 13th IEEE iWEM conference and received the "Finalist Award".



Luqi Chen (Student Member, IEEE) was born in March 2001, Guangzhou, China. She is currently pursuing a Bachelor's degree in the international class of Huizhou University. Her research interests include active and passive reconfigurable intelligent surfaces, miniaturization of power dividers and artificial intelligence. She won the best paper award in the first author category at the 2022 IEEE 5th International Conference on Electronic Information and Communication Technology (ICEICT).