

A Miniaturized Wilkinson Power Divider with Integrated Phase Shifter

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Abstract – This paper reports the design of a compact Wilkinson power divider for use in modern wireless communication systems where circuit size is a critical constraint. The proposed design replaces the conventional quarter-wavelength transmission line with a compact phase-shifting section based on parallel-coupled microstrip lines, providing an impedance transformation factor of $\sqrt{2}$ for proper matching to a 50 Ω system. The power divider is designed to operate at a center frequency of 3.0 GHz on an AD260 substrate, with the phase-shifting function directly integrated into the power-dividing network to reduce the overall circuit footprint. The fabricated prototype occupies an area of 15.367×22.860 mm², corresponding to a size reduction of approximately 22% compared with a conventional Wilkinson power divider. Simulation results obtained using Advanced Design System (ADS) demonstrate strong agreement, with a return loss (S_{11}) better than 15 dB and insertion losses (S_{21} and S_{31}) close to the ideal value of -3 dB at the operating frequency. The fabricated prototype was characterized over the 2–6 GHz frequency range, demonstrating strong agreement with the simulated results. These results indicate that the proposed structure achieves effective power division with good impedance matching while maintaining a compact

size, making it suitable for integration into compact RF and microwave front-end circuits.

Index Terms – Circuit miniaturization, parallel-coupled microstrip lines, phase compensation, Wilkinson power divider.

I. INTRODUCTION

Recent advances in wireless communication technologies have driven the demand for compact, lightweight, and high-performance RF and microwave circuits. Modern applications such as mobile terminals, wearable devices, Internet of Things (IoT) nodes, and vehicle-to-everything (V2X) communication systems require circuit components that not only provide reliable electrical performance but also occupy minimal physical area [1]. As a result, circuit miniaturization has become a key research topic in the development of next-generation wireless front-end systems.

The Wilkinson power divider is a fundamental building block widely used in RF and microwave systems for power distribution, signal combining, and antenna feeding networks. In response to stringent size constraints, numerous miniaturization techniques

Table 1: Summary of reported miniaturization techniques for Wilkinson power dividers

Ref.	Technique	Main Advantage	Limitation
[2]	3-D MMIC integration	Significant size reduction achieved through three-dimensional integration	Complex fabrication process and higher manufacturing cost
[3]	Capacitive loading	Compact circuit realization with reduced physical length	Narrow operating bandwidth
[4]	Active inductors	Effective size reduction using active circuit elements	Additional biasing circuitry and power consumption
[5]	T-shaped transmission lines	Simple planar layout with moderate size reduction	Limited miniaturization capability
[6]	Fractal structure	Harmonic suppression and size reduction	Increased design and optimization complexity
[7]	Resonator-based design	Harmonic control and performance enhancement	Increased layout area compared with simple structures
This work	Coupled-line phase shifter	Compact and planar structure with integrated phase-shifting functionality	Required optimization for impedance and phase balance

for Wilkinson power dividers have been reported in the literature. These include three-dimensional integration technologies [2], lumped-element realizations [8, 9], inductive and capacitive loading methods [3, 4, 10, 11], T-shaped transmission-line configurations [5, 12], fractal-based structures [6], and resonator-assisted designs [1, 7, 13]. While these approaches can effectively reduce circuit size, they often involve trade-offs in bandwidth, fabrication complexity, or design flexibility. A summary of representative miniaturization techniques for Wilkinson power dividers reported in the literature is provided in Table 1. It should be noted that the proposed design employs a lumped capacitor for capacitive compensation, whereas some reported works are based solely on transmission-line structures. The inclusion of a lumped element in this work is intended to provide a simple and practical means for phase adjustment without significantly increasing circuit complexity. Therefore, the comparison focuses on overall design strategy and performance trade-offs rather than strict structural equivalence.

As shown in Table 1, most existing miniaturization approaches achieve size reduction at the expense of increased design complexity, limited bandwidth, or fabrication challenges. This observation motivates the exploration of alternative compact structures that can provide circuit miniaturization while maintaining acceptable electrical performance.

Parallel-coupled microstrip lines have been extensively employed in the realization of compact microwave components, including bandpass filters, impedance transformers, and phase shifters [14–18]. In particular, coupled-line-based phase shifter

configurations, such as Schiffman-type and differential phase shifters, have attracted significant attention due to their planar structure, broadband characteristics, and compatibility with standard fabrication processes. These designs exploit the electromagnetic coupling between adjacent transmission lines to introduce a desired phase delay within a reduced physical length. Despite their advantages, microstrip coupled-line structures inherently suffer from unequal phase velocities between the even and odd propagation modes as a result of dielectric inhomogeneity. This phase imbalance can lead to deviations from the intended phase response, increased insertion loss, and degraded isolation when such structures are integrated into power-dividing or signal-combining networks. To overcome these limitations, a wide range of compensation techniques has been proposed, including capacitive and inductive loading methods, dielectric overlays, and hybrid compensation schemes [19–33]. These approaches provide important design insights for improving the performance of coupled-line-based circuits.

Although a variety of miniaturization techniques have been reported, such as slow-wave structures, defected ground structures (DGS), meandered transmission lines, and lumped-element loading, each approach has certain limitations. For instance, slow-wave and DGS-based techniques often require complex geometrical modifications and may increase fabrication complexity, while lumped-element approaches introduce additional parasitic effects and may limit bandwidth performance. In contrast, the proposed design employs a capacitive-compensated parallel-coupled microstrip structure, which provides a simple planar

implementation without requiring multilayer configurations or intricate layouts. This approach enables effective size reduction while maintaining good impedance matching, power division, and isolation characteristics, making it more suitable for practical RF and microwave circuit integration.

In this work, a compact Wilkinson power divider operating at 3.0 GHz is proposed by replacing the conventional quarter-wavelength transmission line with a 90° phase-shifting section implemented using parallel-coupled microstrip lines. Based on even- and odd-mode analysis, the coupled-line section is designed to provide a characteristic impedance of $1.414Z_0$, enabling the required impedance transformation while occupying a shorter physical length than a traditional $\lambda/4$ line. By integrating the phase-shifting function directly into the power-dividing network, the proposed design achieves circuit miniaturization without significantly compromising electrical performance.

II. DESIGN AND ANALYSIS

A. Design principle of the capacitive compensated coupled-line structure

In RF and microwave circuit design, the physical length of quarter-wavelength ($\lambda/4$) transmission lines often limits circuit miniaturization. To address this issue, a compact phase-shifting structure based on parallel-coupled microstrip lines with capacitive compensation is proposed to emulate the electrical behavior of a conventional quarter-wavelength transmission line.

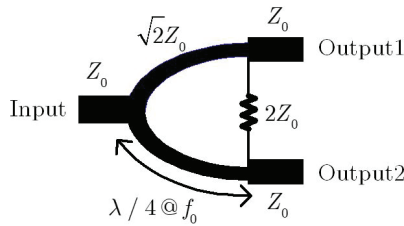


Fig. 1. Conventional Wilkinson power divider with quarter-wavelength transmission lines.

Figure 1 illustrates a conventional Wilkinson power divider, where two $\lambda/4$ transmission lines with characteristic impedance $\sqrt{2}Z_0$ provide impedance matching and equal power division, while an isolation resistor of $2Z_0$ ensures high isolation between output ports. Although excellent electrical performance is achieved, the quarter-wavelength sections result in a relatively large physical footprint.

To achieve size reduction, the proposed design replaces the conventional $\lambda/4$ transmission lines with compact 90° phase-shifting sections, as shown in Fig. 2. Each phase-shifting section is designed to provide an

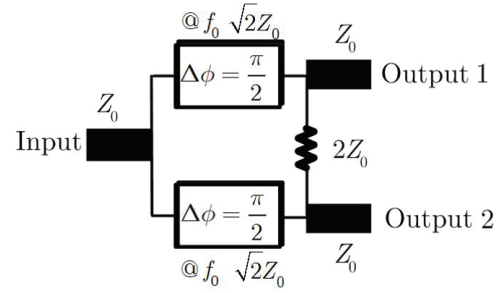


Fig. 2. Proposed Wilkinson power divider using integrated 90° phase-shifting sections.

electrical phase delay of $\pi/2$ and an equivalent characteristic impedance of $\sqrt{2}Z_0$ at the operating frequency f_0 . This approach preserves the required impedance transformation while significantly reducing the circuit size.

The proposed phase-shifting section is realized using a parallel-coupled microstrip line with even- and odd-mode impedances Z_{0e} and Z_{0o} , respectively, and an electrical length $\theta_c < \pi/2$. Due to dielectric inhomogeneity, the even- and odd-mode phase velocities are generally unequal, which degrades circuit performance as in Fig. 3 shows the equivalent two-port network of the capacitive-compensated coupled-line structure. To compensate for this effect, a lumped capacitor with impedance Z_C is connected between the open-circuited ports of the coupled-line section.

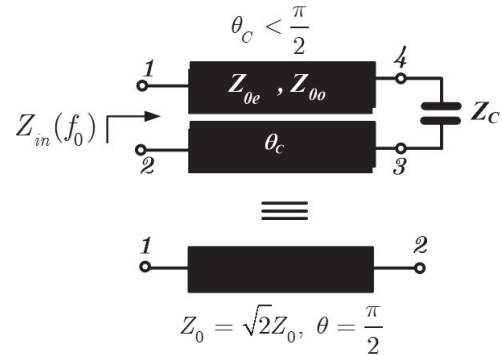


Fig. 3. Equivalent two-port network of the capacitive-compensated coupled-line structure.

For circuit analysis, the coupled-line structure is initially represented as a four-port network. By symmetrically terminating Ports 3 and 4 with shunt capacitive impedances of $Z_C/2$, the network can be reduced to an equivalent symmetric two-port representation, as illustrated in Fig. 4. This shunt capacitive loading primarily introduces an additional phase delay to the odd mode, thereby compensating for the phase velocity mismatch. Physically, the compensation capacitor introduces an additional reactive loading to the coupled-line section,

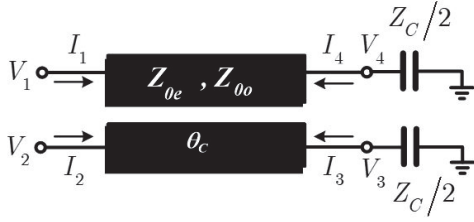


Fig. 4. Voltage-current definition of the capacitive-compensated coupled-line structure for circuit analysis.

which modifies the phase response of the structure. Since the odd mode is more sensitive to the electric-field distribution between the coupled strips, the shunt capacitive loading predominantly affects the odd-mode propagation, introducing an additional phase delay. In contrast, the even mode is comparatively less affected because its field distribution is less concentrated across the coupled region. As a result, the capacitor helps reduce the phase velocity imbalance between the even and odd modes, enabling the shortened coupled-line section to more closely emulate the phase behavior of a conventional quarter-wavelength transmission line.

1. Equivalent two-port impedance representation

Under the assumptions of reciprocity and symmetry, the equivalent two-port impedance parameters of the capacitive-compensated coupled-line structure [29, 33] can be expressed as:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}. \quad (1)$$

Because the proposed structure is geometrically symmetric with respect to the input and output planes and consists of passive reciprocal elements, the impedance matrix exhibits both symmetry and reciprocity [33]. Accordingly, the diagonal elements satisfy $Z_{11} = Z_{22}$ and $Z_{33} = Z_{44}$, whereas the off-diagonal terms follow $Z_{12} = Z_{21}$, $Z_{13} = Z_{24}$, and $Z_{14} = Z_{23}$. Ports 3 and 4 are terminated by shunt capacitive impedances $Z_C/2$, yielding

$$V_3 = -\frac{Z_C}{2} I_3, \quad V_4 = -\frac{Z_C}{2} I_4. \quad (2)$$

By applying the symmetry conditions and imposing the current relationship at Ports 3 and 4 (i.e., $I_4 = -I_3$), the four-port impedance equations can be reduced to

$$\begin{aligned} V_1 &= Z_{11} I_1 + Z_{12} I_2 + (Z_{13} - Z_{14}) I_3, \\ V_2 &= Z_{12} I_1 + Z_{11} I_2 - (Z_{13} - Z_{14}) I_3. \end{aligned} \quad (3)$$

After applying the capacitive boundary conditions and reducing the four-port description to an equivalent

two-port network, the resulting voltage-current relations can be expressed as

$$V_1 = \left(Z_{11} - \frac{(Z_{13} - Z_{14})^2}{Z_C + 2(Z_{11} - Z_{12})} \right) I_1 + \left(Z_{12} + \frac{(Z_{13} - Z_{14})^2}{Z_C + 2(Z_{11} - Z_{12})} \right) I_2, \quad (4)$$

$$V_2 = \left(Z_{12} + \frac{(Z_{13} - Z_{14})^2}{Z_C + 2(Z_{11} - Z_{12})} \right) I_1 + \left(Z_{11} - \frac{(Z_{13} - Z_{14})^2}{Z_C + 2(Z_{11} - Z_{12})} \right) I_2. \quad (5)$$

Equations (4)–(5) indicate that the capacitive-compensated coupled-line section can be represented by an equivalent symmetric two-port Z-parameter matrix. For compactness, define

$$Z_H \triangleq \frac{(Z_{13} - Z_{14})^2}{Z_C + 2(Z_{11} - Z_{12})}. \quad (6)$$

The parameter Z_H represents the effective impedance contribution introduced by the combined effect of the coupling difference and the shunt capacitive loading. Thus, the equivalent two-port representation is written as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} - Z_H & Z_{12} + Z_H \\ Z_{12} + Z_H & Z_{11} - Z_H \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \quad (7)$$

where Z_H captures the combined effect of the coupling imbalance and the shunt capacitive loading, enabling the shortened coupled-line section to emulate a quarter-wavelength impedance inverter at the design frequency.

$$Z_{11T} = Z_{11} - \frac{(Z_{13} - Z_{14})^2}{Z_C + 2(Z_{11} - Z_{12})}, \quad (8)$$

$$Z_{12T} = Z_{12} + \frac{(Z_{13} - Z_{14})^2}{Z_C + 2(Z_{11} - Z_{12})}.$$

Therefore, the equivalent two-port network can be written in matrix form as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11T} & Z_{12T} \\ Z_{12T} & Z_{11T} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \quad (9)$$

Accordingly, the voltage-current relationship of the proposed structure can be written in the standard two-port impedance matrix form as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} - Z_H & Z_{12} + Z_H \\ Z_{12} + Z_H & Z_{11} - Z_H \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \quad (10)$$

The parameter Z_H represents the combined effect of coupling imbalance and shunt capacitive loading,

enabling the shortened coupled-line section to emulate a quarter-wavelength impedance inverter.

2. Input matching condition

From the equivalent two-port impedance matrix in (10), the input reflection coefficient can be expressed in terms of the Z-parameters as [29, 33]

$$S_{11} = \frac{(Z_{11T} - Z_0)^2 - Z_{12T}^2}{(Z_{11T} + Z_0)^2 - Z_{12T}^2}. \quad (11)$$

The input reflection coefficient of the equivalent two-port network is given by

$$S_{11} = \frac{(Z_{11T} - Z_0)^2 - Z_{12T}^2}{(Z_{11T} + Z_0)^2 - Z_{12T}^2}. \quad (12)$$

Perfect input matching at the design frequency f_0 is achieved when $S_{11}(f_0) = 0$, which yields a closed-form expression for the required capacitive impedance Z_C .

3. Physical design parameters

The required shunt capacitance can be obtained from

$$C_p = \frac{Z_0}{2\omega_0 |\text{Im}(Z_C)|}, \quad (13)$$

where $\omega_0 = 2\pi f_0$. The electrical length of the shortened coupled-line section is determined by

$$\theta_f = \frac{1}{\pi k} \tan^{-1} \left(\frac{2Z_{0o}}{\sqrt{4Z_{0o}^2 - Z_C^2}} \right), \quad (14)$$

with

$$k = \sqrt{\frac{\epsilon_{\text{effo}}}{\epsilon_{\text{effe}}}}, \quad (15)$$

representing the phase velocity ratio between the odd and even modes.

4. Transmission performance

Finally, the transmission coefficient of the synthesized two-port network is expressed as

$$S_{21} = \frac{2Z_0 Z_{12T}}{(Z_{11T} + Z_0)^2 - Z_{12T}^2}, \quad (16)$$

or equivalently,

$$S_{21} = \frac{2Z_0(Z_{12} + Z_H)}{(Z_{11} - Z_H + Z_0)^2 - (Z_{12} + Z_H)^2}. \quad (17)$$

Equation (17) confirms that the transmission performance of the proposed capacitive-compensated coupled-line structure is directly governed by the synthesized impedance parameter Z_H , enabling equal power division while maintaining a compact circuit footprint.

B. Impedance transformation and electrical length adjustment of the capacitive-compensated parallel-coupled transmission line

To quantitatively describe the compensation behavior, the synthesized values of the shunt capacitance C_p and the shortened electrical length θ_f were extracted for coupling levels ranging from -14 to -8 dB. The coupling range from -8 to -14 dB was selected because it represents a practical design interval for parallel-coupled microstrip lines at 3.0 GHz, where the coupling strength is sufficiently high to support compact phase-shifter implementation while still maintaining realizable physical dimensions and acceptable fabrication tolerance.

In addition to circuit miniaturization, the proposed capacitive-compensated parallel-coupled transmission line must simultaneously satisfy two essential design requirements: impedance transformation and precise electrical length control. In a conventional Wilkinson power divider, each quarter-wavelength ($\lambda/4$) transmission line provides both a 90° phase shift and an impedance transformation from Z_0 to $\sqrt{2}Z_0$. When the physical length of the transmission line is reduced, these two functions must be preserved through appropriate circuit synthesis. In the proposed structure, the impedance transformation is achieved through the even- and odd-mode characteristic impedances of the parallel-coupled microstrip lines. By properly selecting Z_{0e} and Z_{0o} , the coupled-line section can be designed to exhibit an equivalent characteristic impedance of $\sqrt{2}Z_0$ at the operating frequency. This behavior emulates the impedance-inverting property of a conventional quarter-wavelength transmission line while occupying a shorter physical length. However, due to dielectric inhomogeneity in microstrip structures, the even- and odd-mode phase velocities are generally unequal, causing a deviation from the desired 90° electrical phase shift. To compensate for this effect, a shunt capacitor C_p is introduced between the open-circuited ends of the coupled-line section. The capacitive loading effectively introduces an additional phase delay to the odd-mode propagation, while the even mode remains comparatively unaffected. As a result, the overall phase imbalance between the two modes is reduced. By appropriately selecting the value of the shunt capacitance C_p , the shortened coupled-line section can be adjusted to provide an exact 90° electrical phase shift at the design frequency f_0 , despite its reduced physical length. Consequently, the capacitive-compensated coupled-line structure simultaneously achieves impedance transformation and electrical length control, enabling it to serve as an electrically equivalent substitute for a conventional quarter-wavelength transmission line in compact Wilkinson power divider applications. To facilitate practical implementation, the design equations derived

in the previous subsection are employed to determine suitable initial values for the physical and electrical parameters of the proposed structure. Specifically, the even- and odd-mode impedances, the shortened electrical length, and the shunt capacitance C_p are jointly considered to ensure that both impedance matching and phase compensation conditions are satisfied at the operating frequency f_0 . In the synthesis procedure, the coupled-line geometry is first selected to achieve the required coupling coefficient, which directly governs the values of Z_{0e} and Z_{0o} . The physical dimensions of the coupled lines, including the conductor width W , spacing S , and coupling length L , are then adjusted accordingly based on the chosen substrate parameters. In this work, the proposed structures are implemented on FR4 and AD260 substrates in order to investigate the influence of dielectric properties on the impedance transformation and phase response. After defining the coupled-line geometry, the shunt capacitive loading C_p is introduced to compensate for the phase velocity mismatch between the even and odd modes. The value of C_p is initially estimated using the derived closed-form expressions and subsequently refined through parametric optimization. The optimization process focuses on minimizing the input reflection coefficient S_{11} while maintaining a transmission coefficient S_{21} close to -3 dB and achieving a phase shift of approximately 90° at the design frequency. The electrical performance of the synthesized two-port network is evaluated in terms of its scattering parameters, namely S_{11} , S_{21} , and the phase of S_{21} . These parameters provide direct insight into the impedance matching, insertion loss, and phase characteristics of the proposed structure. By systematically adjusting the coupled-line dimensions and the shunt capacitance C_p , an optimal trade-off between size reduction and electrical performance can be achieved. To further elucidate the impedance transformation and phase compensation mechanism, Figs. 5–7 present the parametric synthesis results obtained for the FR4 substrate ($\epsilon_r = 4.55$). Figure 5 illustrates the variation of the required shunt capacitance C_p and the shortened electrical length θ_f as functions of the coupling factor. As the magnitude of the coupling factor decreases (from -8 to -14 dB), the required compensation capacitance is reduced, while the effective electrical length shifts closer to the ideal 90° condition. In general, stronger coupling requires a larger compensation capacitance and a corresponding adjustment of the electrical length to maintain the desired impedance transformation and phase response.

This behavior confirms that stronger electromagnetic coupling requires greater capacitive loading to mitigate the even–odd mode phase imbalance. Figure 6 presents the evolution of the even- and odd-mode impedances before and after optimization. It can be

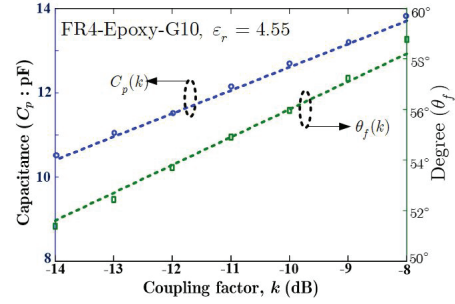


Fig. 5. Relationship between shunt capacitance C_p , shortened electrical length θ_f , and coupling factor for the FR4 substrate ($\epsilon_r = 4.55$).

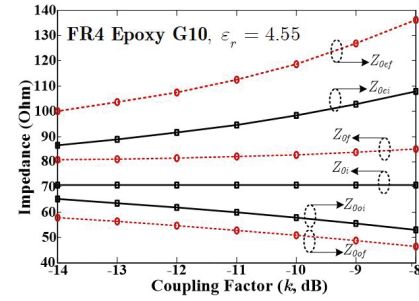


Fig. 6. Initial and optimized even- and odd-mode impedances versus coupling factor for the FR4 substrate.

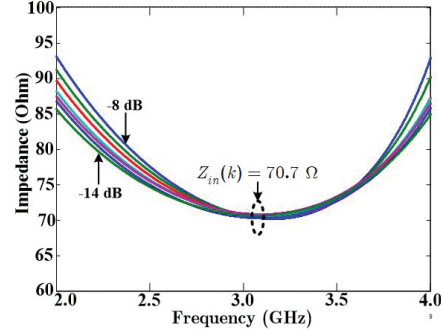


Fig. 7. Input impedance Z_{in} versus frequency for different coupling factors on the FR4 substrate.

observed that the optimized values gradually approach the required impedance transformation condition of $\sqrt{2}Z_0$, ensuring that the synthesized section functions as an equivalent quarter-wavelength impedance inverter. Finally, Fig. 7 shows the input impedance response of the synthesized structure over frequency. All coupling scenarios exhibit an impedance minimum near 70.7Ω at 3.0 GHz, validating that the proposed structure successfully preserves the impedance-inverting property at the design frequency. The corresponding synthesized design parameters for the FR4 substrate are summarized in Table 2. The table presents the initial and optimized

Table 2: Design parameters of the capacitive-compensated parallel-coupled transmission line implemented on FR4 substrate at 3.0 GHz for various coupling levels

Coupling (dB)	Initial Impedance (Z_0, Z_{0e}, Z_{0o})	Initial Dimensions (W, S, L) [mm]	Optimized Impedance (Z_0, Z_{0e}, Z_{0o})	Optimized Dimensions (W, S, L) [mm]	C_p and θ_f
-8.0	$Z_0 = 70.70$ $Z_{0e} = 107.75$ $Z_{0o} = 46.38$	$W = 1.13$ $S = 0.34$ $L = 7.19$	$Z_0 = 59.48$ $Z_{0e} = 86.94$ $Z_{0o} = 40.70$	$W = 1.71$ $S = 0.34$ $L = 8.98$	$C_p = 13.82$ pF $\theta_f = 58.8^\circ$
-9.0	$Z_0 = 70.70$ $Z_{0e} = 102.45$ $Z_{0o} = 48.79$	$W = 1.21$ $S = 0.45$ $L = 7.15$	$Z_0 = 60.46$ $Z_{0e} = 84.75$ $Z_{0o} = 43.13$	$W = 1.74$ $S = 0.45$ $L = 8.84$	$C_p = 13.14$ pF $\theta_f = 57.62^\circ$
-10.0	$Z_0 = 70.70$ $Z_{0e} = 98.09$ $Z_{0o} = 50.95$	$W = 1.27$ $S = 0.57$ $L = 7.11$	$Z_0 = 61.27$ $Z_{0e} = 82.90$ $Z_{0o} = 45.29$	$W = 1.76$ $S = 0.57$ $L = 8.71$	$C_p = 12.69$ pF $\theta_f = 55.87^\circ$
-11.0	$Z_0 = 70.70$ $Z_{0e} = 94.45$ $Z_{0o} = 52.91$	$W = 1.32$ $S = 0.71$ $L = 7.08$	$Z_0 = 61.76$ $Z_{0e} = 80.78$ $Z_{0o} = 47.21$	$W = 1.79$ $S = 0.71$ $L = 8.57$	$C_p = 12.15$ pF $\theta_f = 54.90^\circ$
-12.0	$Z_0 = 70.70$ $Z_{0e} = 91.38$ $Z_{0o} = 54.69$	$W = 1.37$ $S = 0.86$ $L = 7.06$	$Z_0 = 62.20$ $Z_{0e} = 79.02$ $Z_{0o} = 48.96$	$W = 1.81$ $S = 0.86$ $L = 8.45$	$C_p = 11.51$ pF $\theta_f = 53.80^\circ$
-13.0	$Z_0 = 70.70$ $Z_{0e} = 88.78$ $Z_{0o} = 56.30$	$W = 1.40$ $S = 1.02$ $L = 7.04$	$Z_0 = 62.64$ $Z_{0e} = 77.58$ $Z_{0o} = 50.58$	$W = 1.82$ $S = 1.02$ $L = 8.37$	$C_p = 11.05$ pF $\theta_f = 52.83^\circ$
-14.0	$Z_0 = 70.70$ $Z_{0e} = 86.54$ $Z_{0o} = 57.75$	$W = 1.42$ $S = 1.19$ $L = 7.02$	$Z_0 = 62.96$ $Z_{0e} = 76.23$ $Z_{0o} = 52.01$	$W = 1.83$ $S = 1.19$ $L = 8.29$	$C_p = 10.51$ pF $\theta_f = 52.09^\circ$

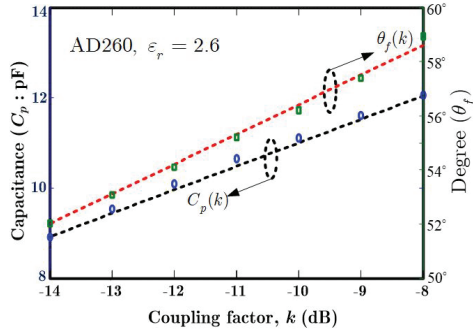


Fig. 8. Variation of compensation capacitance C_f and shortened electrical length θ_f versus coupling factor for the AD260 substrate ($\epsilon_r = 2.6$).

even- and odd-mode impedances, physical dimensions, compensation capacitance, and shortened electrical length for coupling levels ranging from -8 to -14 dB. It can be observed that stronger coupling requires a larger compensation capacitance and a longer electrical length adjustment to satisfy the impedance transformation and phase compensation requirements. Similarly, Figs. 8–10 present the corresponding parametric results for the AD260 substrate ($\epsilon_r = 2.6$). Compared with

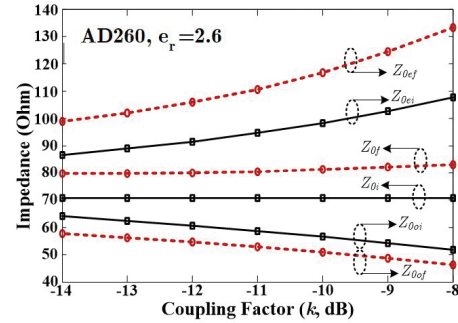
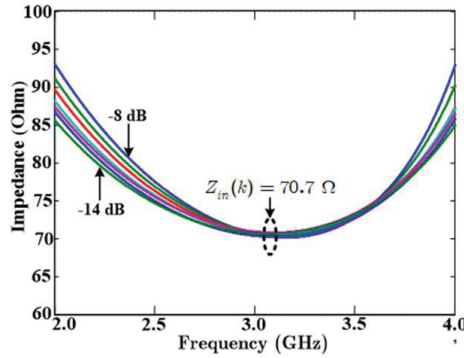


Fig. 9. Initial and optimized even- and odd-mode impedances versus coupling factor for the AD260 substrate.

FR4, the lower dielectric constant of AD260 modifies the even-odd mode field distribution, leading to slightly different compensation capacitance values and electrical lengths. Nevertheless, the same monotonic trend between coupling strength and required capacitive loading is clearly preserved. As shown in Fig. 9, the optimized even- and odd-mode impedances converge toward the target impedance transformation condition of $\sqrt{2}Z_0$, confirming that the proposed synthesis method

Table 3: Design parameters of the capacitive-compensated parallel-coupled transmission line implemented on AD260 substrate at 3.0 GHz for various coupling levels

Coupling (dB)	Initial Impedance (Z_0, Z_{0e}, Z_{0o})	Initial Dimensions (W, S, L) [mm]	Optimized Impedance (Z_0, Z_{0e}, Z_{0o})	Optimized Dimensions (W, S, L) [mm]	Compensation (C_p, θ_f)
-8	$Z_0 = 70.70$ $Z_{0e} = 107.75$ $Z_{0o} = 46.38$	$W = 1.13$ $S = 0.34$ $L = 7.19$	$Z_0 = 59.48$ $Z_{0e} = 86.94$ $Z_{0o} = 40.70$	$W = 1.71$ $S = 0.34$ $L = 8.98$	$C_p = 12.04$ pF $\theta_f = 58.9^\circ$
-9	$Z_0 = 70.70$ $Z_{0e} = 102.45$ $Z_{0o} = 48.79$	$W = 1.21$ $S = 0.45$ $L = 7.15$	$Z_0 = 60.46$ $Z_{0e} = 84.75$ $Z_{0o} = 43.13$	$W = 1.74$ $S = 0.45$ $L = 8.84$	$C_p = 11.62$ pF $\theta_f = 57.34^\circ$
-10	$Z_0 = 70.70$ $Z_{0e} = 98.09$ $Z_{0o} = 50.95$	$W = 1.27$ $S = 0.57$ $L = 7.11$	$Z_0 = 61.27$ $Z_{0e} = 82.90$ $Z_{0o} = 45.29$	$W = 1.76$ $S = 0.57$ $L = 8.71$	$C_p = 11.12$ pF $\theta_f = 56.08^\circ$
-11	$Z_0 = 70.70$ $Z_{0e} = 94.45$ $Z_{0o} = 52.91$	$W = 1.32$ $S = 0.71$ $L = 7.08$	$Z_0 = 61.76$ $Z_{0e} = 80.78$ $Z_{0o} = 47.21$	$W = 1.79$ $S = 0.71$ $L = 8.57$	$C_p = 10.87$ pF $\theta_f = 54.92^\circ$
-12	$Z_0 = 70.70$ $Z_{0e} = 91.38$ $Z_{0o} = 54.69$	$W = 1.37$ $S = 0.86$ $L = 7.06$	$Z_0 = 62.20$ $Z_{0e} = 79.02$ $Z_{0o} = 48.96$	$W = 1.81$ $S = 0.86$ $L = 8.45$	$C_p = 10.12$ pF $\theta_f = 53.92^\circ$
-13	$Z_0 = 70.70$ $Z_{0e} = 88.78$ $Z_{0o} = 56.30$	$W = 1.40$ $S = 1.02$ $L = 7.04$	$Z_0 = 62.64$ $Z_{0e} = 77.58$ $Z_{0o} = 50.58$	$W = 1.82$ $S = 1.02$ $L = 8.37$	$C_p = 9.55$ pF $\theta_f = 53.11^\circ$
-14	$Z_0 = 70.70$ $Z_{0e} = 86.54$ $Z_{0o} = 57.75$	$W = 1.42$ $S = 1.19$ $L = 7.02$	$Z_0 = 62.96$ $Z_{0e} = 76.23$ $Z_{0o} = 52.01$	$W = 1.83$ $S = 1.19$ $L = 8.29$	$C_p = 8.93$ pF $\theta_f = 52.38^\circ$

Fig. 10. Input impedance Z_{in} versus frequency for different coupling levels on the AD260 substrate.

is applicable to substrates with different dielectric constants. Finally, Fig. 10 confirms that the input impedance remains approximately 70.7Ω at 3.0 GHz for all investigated coupling levels. This validates that the impedance-inverting property and phase compensation mechanism of the proposed capacitive-compensated coupled-line structure is robust with respect to substrate variation. The corresponding design parameters obtained for the AD260 substrate are listed in Table 3. Similar trends can

be observed, where the required compensation capacitance and electrical length vary systematically with the coupling level. Compared with the FR4 substrate, the lower dielectric constant of AD260 results in slightly different optimized impedance values and compensation requirements while maintaining the desired impedance transformation characteristics at 3 GHz.

C. Impedance transformation and electrical length adjustment

To quantitatively describe the compensation behavior, the synthesized values of the shunt capacitance C_p and the shortened electrical length θ_f were extracted for coupling levels ranging from -14 to -8 dB. Using the parametric data obtained from Fig. 5, a linear curve-fitting procedure was performed to establish approximate analytical relationships between the coupling factor k (in dB), the required compensation capacitance, and the corresponding shortened electrical length. The fitted expressions are obtained as

$$C_p(k) = 0.55k + 18 \quad (\text{pF}), \quad (18)$$

$$\theta_f(k) = 1.2k + 68 \quad (\text{degree}), \quad (19)$$

where k denotes the coupling factor in decibels (dB). Equations (18) and (19) indicate that both the compensation capacitance and the shortened electrical length exhibit an approximately linear dependence on the coupling level within the investigated design range. Specifically, as the magnitude of the coupling factor decreases (i.e., weaker coupling), the required shunt capacitance is reduced, while the electrical length shifts closer to the ideal 90° condition. This behavior confirms that stronger coupling requires greater capacitive loading to compensate for the even-odd mode phase velocity imbalance. It should be noted that the above expressions are valid within the coupling range of $-14 \leq k \leq -8$ dB and are intended to serve as practical design guidelines for rapid initial parameter estimation prior to full-wave optimization. In addition to the compensation capacitance and electrical length, Fig. 9 also reveals an approximately linear relationship between the coupling factor and the even- and odd-mode characteristic impedances for the AD260 substrate. By applying linear curve fitting within the range $-14 \leq k \leq -8$ dB, the following empirical expressions are obtained:

$$C_p(k) = 0.52k + 16 \quad (\text{pF}), \quad (20)$$

$$\theta_f(k) = 1.1k + 67 \quad (\text{degree}), \quad (21)$$

at the design frequency of 3.0 GHz, as verified in Fig. 10. This result confirms that the proposed capacitive-compensated coupled-line section preserves the impedance-inverting property of a conventional quarter-wavelength transformer while enabling substantial physical length reduction. The impedance transformation and electrical length adjustment of the modified parallel-coupled transmission line can be achieved by appropriately tuning the circuit parameters and introducing a compensating shunt capacitor. The graphical results confirm the relationship between the electrical parameters and the corresponding frequency response obtained from both simulation and experimental measurements.

This study focuses on the impedance transformation and phase adjustment of a microstrip parallel-coupled transmission line with its open ends terminated by a compensating capacitor (C_p). The investigation was conducted at an operating frequency of 3.0 GHz on FR4 and AD260 substrates in order to enhance the transmission-line characteristics, including phase shift and impedance transformation performance. The circuit synthesis and parameter optimization were carried out using parallel-coupled microstrip lines implemented on FR4 and AD260 printed circuit boards. The coupling coefficient was varied within the range of -8 to -14 dB to examine its influence on the required compensation capacitance and electrical phase response.

By systematically adjusting the coupled-line dimensions and the compensation capacitor C_p , the modified structure can be synthesized to exhibit improved phase accuracy and effective impedance transformation at the design frequency. The results demonstrate that proper capacitive compensation enables the shortened coupled-line section to emulate the electrical behavior of a conventional quarter-wavelength transmission line while maintaining a reduced physical size.

III. MATERIALS AND METHODS

A. Proposed circuit configuration

The proposed miniaturized Wilkinson power divider is illustrated in Fig. 11. Unlike the conventional design employing quarter-wavelength transmission lines, the proposed structure integrates a capacitive-compensated parallel-coupled microstrip section to simultaneously achieve impedance transformation and phase shifting. Each branch consists of a shortened coupled-line section characterized by even- and odd-mode impedances (Z_{0e}, Z_{0o}) and electrical length θ_c , with a compensating capacitor C_p connected at the open ends. An isolation resistor of $2Z_0$ is placed between the output ports, preserving the Wilkinson isolation property. The design is targeted for operation at 3.0 GHz with a system impedance of $Z_0 = 50 \Omega$.

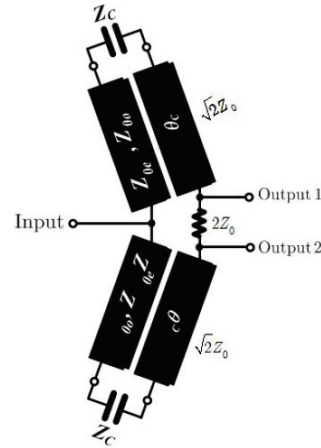


Fig. 11. Proposed miniaturized Wilkinson power divider using capacitive-compensated parallel-coupled transmission lines.

B. Circuit simulation and results

The schematic model of the proposed miniaturized Wilkinson power divider was implemented in Advanced Design System (ADS) 2022 Update 1 (Keysight Technologies), [34], as illustrated in Fig. 12. The substrate parameters were defined using the MSUB (microstrip substrate) block, including the relative dielectric constant, substrate thickness,

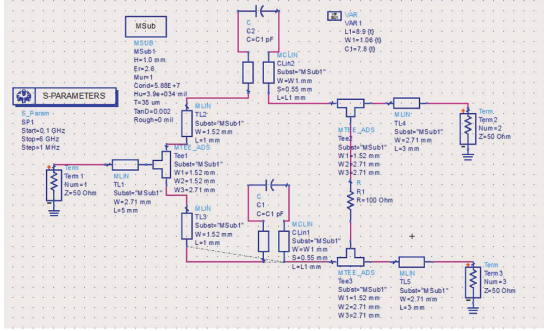


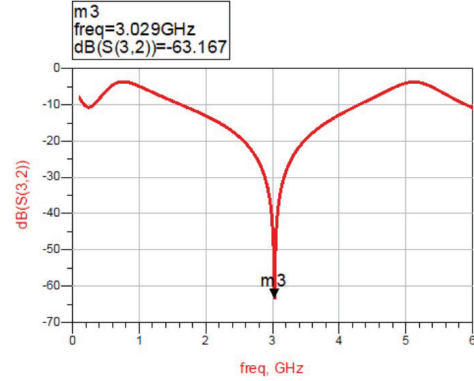
Fig. 12. ADS schematic of the proposed Wilkinson power divider including substrate definition, coupled-line sections, and compensation capacitor.

conductor thickness, and loss tangent corresponding to the AD260 substrate. The coupled-line sections were modeled using microstrip coupled-line elements (MCLIN), while the single transmission lines were implemented using MLIN (microstrip line) components. The shunt compensation capacitor C_p was realized as a lumped capacitor connected between the open-circuited ends of the coupled-line section. A $100\ \Omega$ isolation resistor was placed between the output ports to preserve the inherent isolation property of the conventional Wilkinson topology. S-parameter simulations were performed using the S.Param block in ADS over a frequency range from 0.1 GHz to 6 GHz with a frequency resolution of 1 MHz. All ports were terminated with a reference impedance of $50\ \Omega$ to ensure compatibility with standard microwave measurement conditions.

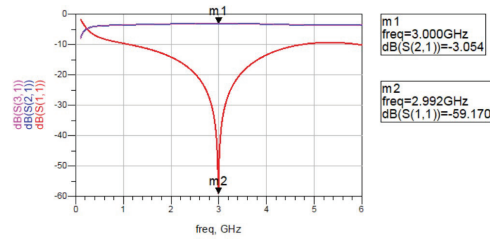
Parametric optimization was conducted to simultaneously adjust the physical dimensions (W, S, L) and the compensation capacitance C_p in order to achieve: (i) proper input impedance matching, (ii) equal power division, and (iii) an electrical phase condition of approximately 90° at the design frequency of 3.0 GHz. The optimization was performed using a combination of parameter sweep, manual tuning, and iterative adjustment to achieve the desired matching, power division, and phase response at 3.0 GHz.

The simulated scattering parameters of the optimized design are presented in Fig. 13. At the center frequency of 3.0 GHz, the proposed power divider exhibits an insertion loss of approximately $-3.05\ \text{dB}$, which is very close to the theoretical value of $-3\ \text{dB}$ for ideal equal power division.

The input return loss is better than 50 dB, indicating excellent impedance matching at the design frequency. Moreover, the isolation between the output ports (S_{23}) is better than 60 dB, confirming that the compensated coupled-line structure successfully maintains the isolation performance of the conventional Wilkinson divider despite the reduced physical length.



(a)



(b)

Fig. 13. Simulated S-parameters of the proposed Wilkinson power divider. (a) Isolation characteristic. (b) Return loss and insertion loss.

C. Fabrication and measurement procedure

After circuit and electromagnetic (EM) optimization, the final layout was exported from ADS and fabricated using a standard printed circuit board (PCB) photolithography process. The microstrip patterns were etched on FR4 and AD260 substrates. For clarity, the AD260 substrate used in this work has a relative dielectric constant of $\epsilon_r = 2.6$, a thickness of 1 mm, and a copper thickness of $35\ \mu\text{m}$.

The compensation capacitor C_p was implemented using a commercial surface-mount chip capacitor soldered between the open ends of the parallel-coupled microstrip lines. The chip capacitor used in the prototype has a tolerance of $\pm 5\%$, which may introduce slight variations in the measured results compared with the simulated values.

A $100\ \Omega$ surface-mount chip resistor was used to realize the isolation resistor between the two output ports, thereby preserving the intrinsic isolation characteristic of the Wilkinson topology.

Standard $50\ \Omega$ SMA (Sub-miniature version A) connectors were mounted at the input and output ports. Particular care was taken during soldering to minimize parasitic inductance and excess conductor loss at the feed transitions, which may otherwise degrade the high-frequency performance.

Table 4: Design parameters of the proposed miniaturized Wilkinson power divider implemented on AD260 substrate at 3.0 GHz

Substrate Parameters (AD260)			
$\epsilon_r = 2.6$	$W_{50} = 2.71 \text{ mm}$	$W_{70.7} = 1.52 \text{ mm}$	$f_0 = 3.0 \text{ GHz}$
Coupled-Line Design Parameters			
Coupling factor C	$Z_0 = 61.96 \text{ }\Omega$	$Z_{0e} = 102.95 \text{ }\Omega$	$Z_{0o} = 61.96 \text{ }\Omega$
-12.09 dB	$K_E = 2.142$	$K_O = 1.819$	
Physical dimensions		$W = 1.06 \text{ mm}, S = 0.55 \text{ mm}, L = 13.3 \text{ mm}$	
Optimized Values			
Compensation capacitor	$C_p = 7.8 \text{ pF}$		
Optimized dimensions	$W = 1.06 \text{ mm}, S = 0.55 \text{ mm}, L = 8.9 \text{ mm}$		
Simulated S-Parameters at 3.0 GHz			
$S_{21} = S_{31}$	-3.05 dB	$S_{11} = -59.17 \text{ dB}$	$S_{23} = -63 \text{ dB}$
Operational bandwidth: 2–6 GHz			

The fabricated prototype was characterized using a calibrated vector network analyzer (VNA) over the frequency range of 2.0–6.0 GHz. Prior to measurement, a full two-port Short-Open-Load-Through (SOLT) calibration was performed. The calibration reference plane was established at the SMA connector interfaces to eliminate systematic errors caused by cables, connectors, and adapters.

The measured S-parameters were subsequently compared with the circuit-level and EM simulation results. Any minor discrepancies are attributed to fabrication tolerances, variations in substrate dielectric properties, and parasitic effects of lumped components.

Table 4 summarizes the key design parameters of the proposed miniaturized Wilkinson power divider implemented on the AD260 substrate at 3.0 GHz. The table presents the initial coupled-line parameters, optimized physical dimensions, and the selected compensation capacitance. It can be observed that the coupling factor of -12.09 dB results in optimized even- and odd-mode impedances that satisfy the impedance transformation requirement of approximately $\sqrt{2}Z_0$. After compensation, the electrical length is shortened from the conventional quarter-wavelength condition, while maintaining excellent impedance matching and isolation performance.

The fabricated prototype of the proposed miniaturized Wilkinson power divider is shown in Fig. 14. The microstrip layout was implemented on the AD260 substrate with a three-port configuration and integrated parallel-coupled transmission-line sections. The overall physical dimensions of the fabricated circuit are approximately $15.4 \times 22.9 \text{ mm}^2$, corresponding to a size reduction of about 22% compared with a conventional quarter-wavelength Wilkinson power divider operating at the same frequency. Surface-mount compensation capacitors were soldered between the open-circuited

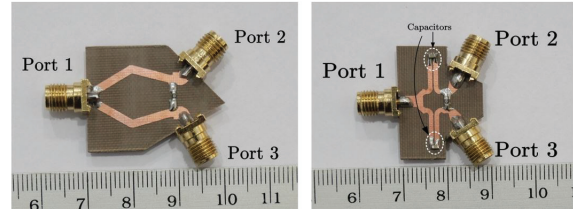


Fig. 14. Fabricated prototype of the proposed miniaturized Wilkinson power divider.

ends of the coupled-line structure, while a 100Ω isolation resistor was mounted between the output ports to preserve the Wilkinson topology. The experimental realization confirms that the proposed capacitive-compensated coupled-line structure can be implemented using standard single-layer PCB fabrication without requiring multilayer processing or three-dimensional integration. The compact planar configuration makes the design suitable for integration into modern RF front-end modules.

IV. RESULTS AND DISCUSSION

The measured S-parameters of the fabricated prototypes, including both the proposed miniaturized design and the conventional quarter-wavelength Wilkinson power divider, were obtained using a calibrated vector network analyzer (Keysight S5065) over the frequency range of 2.0–6.0 GHz.

A. S-parameter performance

Figure 15 compares the measured S-parameters of the proposed and conventional structures. At the design frequency of 3.0 GHz, the proposed miniaturized power divider exhibits S_{21} and S_{31} of approximately -3.2 dB , which are very close to the ideal -3 dB value for equal

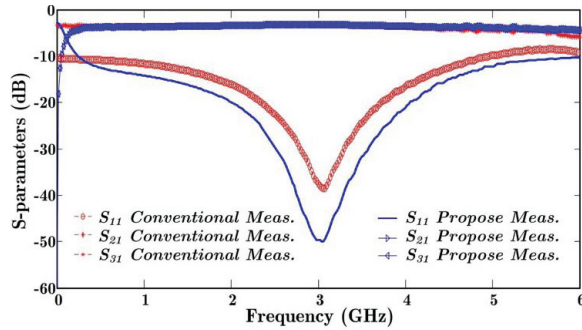


Fig. 15. Measured S-parameters of the proposed and conventional Wilkinson power dividers over the frequency range of 2.0–6.0 GHz.

power division. The slight additional loss compared to simulation is attributed to dielectric loss of the AD260 substrate, conductor loss, soldering parasitics, and SMA connector effects. The measured input return loss S_{11} is better than 20 dB at 3.0 GHz, indicating good impedance matching performance. Although the simulated return loss was below -50 dB, the measured result reflects practical implementation conditions. Compared with the conventional design, the proposed structure maintains comparable power division characteristics, while achieving a significant size reduction of approximately 22%. This confirms that the capacitive-compensated coupled-line section effectively replaces the conventional quarter-wavelength transmission line without degrading fundamental performance.

B. Phase difference analysis

In addition to amplitude characteristics, the phase response between the two output ports was also investigated. Figure 16 shows the measured phase difference

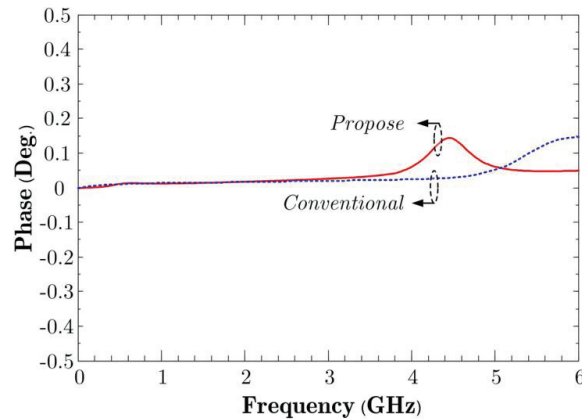


Fig. 16. Measured phase difference between output ports of the proposed and conventional Wilkinson power dividers.

between the output ports for both the proposed and conventional structures. Near the operating frequency of 3.0 GHz, the proposed design maintains a phase condition very close to the desired 90° relationship, demonstrating that the capacitive compensation successfully mitigates the even–odd mode phase velocity imbalance inherent in microstrip coupled-line structures. Across the wider frequency range of 2.0–6.0 GHz, the proposed structure exhibits a stable and controlled phase variation, while preserving performance comparable to the conventional topology. This confirms that the shortened coupled-line section provides accurate electrical-length equivalence to the $\lambda/4$ transmission line. Overall, good agreement between theoretical analysis, simulation, and measurement is observed. The proposed capacitive-compensated parallel-coupled transmission-line structure achieves accurate impedance transformation, controlled phase response, and approximately 22% size reduction, making it suitable for compact RF front-end applications.

C. Discussion

For a clearer quantitative comparison, the measured performance of the conventional quarter-wavelength Wilkinson power divider and the proposed miniaturized design is summarized as follows. At the design frequency of 3.0 GHz, the conventional structure exhibits an input return loss S_{11} of approximately -39 dB, whereas the proposed design achieves an improved return loss of about -50 dB. This indicates that the capacitive-compensated coupled-line section provides more accurate impedance transformation at the operating frequency. Regarding power division performance, the conventional divider shows S_{21} and S_{31} of approximately -3.27 dB, while the proposed structure achieves -3.25 dB for both output ports. The difference between the two designs is negligible (less than 0.02 dB), confirming that the miniaturization technique does not degrade equal power division characteristics. In terms of physical dimensions, the conventional design occupies an area of $16.306 \times 27.584 \text{ mm}^2$, whereas the proposed structure measures $15.367 \times 22.860 \text{ mm}^2$. This corresponds to an overall footprint reduction of approximately 22%. The size reduction is achieved without compromising impedance matching or insertion-loss performance. These results demonstrate that the proposed capacitive-compensated parallel-coupled transmission-line structure successfully replaces the conventional quarter-wavelength section, providing improved matching performance together with significant circuit miniaturization. It should be noted that the potential coupling effects between adjacent microstrip lines were considered in the design. The

Table 5: Performance comparison with representative compact Wilkinson power dividers

Ref.	Frequency (GHz)	Technique	Key Feature	Limitation
[1]	3.0	Resonator-based	Harmonic suppression	Complex structure
[3]	2.0	Capacitive loading	Compact design	Lumped elements required
[4]	2.4	Active inductors	Size reduction	High complexity
[11]	2.45	Stub-based	Compact structure	Limited flexibility
[6]	0.9	DGS / Fractal	Size reduction	Ground modification required
This work	3.0	Coupled-line + capacitor	Compact + integrated phase	Simple planar structure

spacing between transmission lines was carefully optimized to minimize unintended parasitic coupling. Furthermore, full-wave EM simulation inherently accounts for these coupling effects. The good agreement between simulation and measurement confirms that such effects have negligible impact on the overall performance.

The performance of the coupled microstrip line used in the proposed design can be compared with that of a conventional quarter-wavelength transmission line. In the proposed structure, the phase response is achieved through the combined effect of electromagnetic coupling and capacitive compensation, enabling the shortened transmission line to approximate the required 90° phase shift at the design frequency. In terms of insertion loss, the coupled-line section with a lumped capacitor may introduce slightly higher loss compared to a conventional uniform transmission line due to additional coupling effects and component parasitics. However, both simulated and measured results indicate that the insertion loss remains close to the ideal value, demonstrating that the additional loss is minimal. These results confirm that the proposed approach provides an effective trade-off between size reduction and electrical performance, making it suitable for compact RF and microwave circuit applications.

Table 5 compares the proposed design with representative compact Wilkinson power dividers reported in the literature. Various techniques such as resonator-based structures, capacitive loading, DGS, and stub-based configurations have been widely used to achieve size reduction. However, these approaches often introduce additional structural complexity or require modifications to the ground plane or active components. In contrast, the proposed design employs a capacitive-compensated coupled-line structure, which enables size reduction through phase integration while maintaining a simple planar configuration. This makes the proposed design more suitable for practical implementation in RF and microwave circuits.

V. CONCLUSIONS

A compact Wilkinson power divider employing a capacitive-compensated parallel-coupled microstrip transmission-line section has been presented. The conventional quarter-wavelength transmission line was replaced by a shortened coupled-line structure integrated with a shunt compensation capacitor, enabling simultaneous impedance transformation and precise 90° phase control at 3.0 GHz. Based on even-odd mode analysis, closed-form expressions were derived to determine the required compensation capacitance and shortened electrical length. Parametric investigation further revealed an approximately linear relationship between the coupling factor and both the compensation capacitance and phase response, providing practical design guidelines within the range of -14 to -8 dB.

The proposed divider was designed using Advanced Design System (ADS), fabricated on an AD260 substrate, and experimentally characterized using a calibrated vector network analyzer over the frequency range of 2.0–6.0 GHz. At the operating frequency of 3.0 GHz, the measured S_{21} and S_{31} were approximately -3.2 dB, the return loss exceeded 20 dB, and the isolation was better than 30 dB. These results show good agreement with simulation and confirm accurate impedance transformation and phase compensation. Compared with the conventional quarter-wavelength Wilkinson power divider, the proposed structure achieves approximately 22% reduction in physical area while preserving balanced power division and isolation characteristics. The fully planar configuration, together with the simple capacitive compensation technique, makes the design suitable for compact RF and microwave front-end applications.

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