Modeling of Via Interconnect through Pad in Printed Circuit Board

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Abstract ─ In this paper the methods of finding inductance L of a cylindrical via and capacitance C due to via pad in printed circuit board (PCB) are described. Initially a thin cylindrical via of diameter d without pad is connected between a 50 ohm copper trace on the top of a dielectric substrate and a ground plane at the bottom. The line is terminated with matched load. The geometrical structure is simulated using Ansoft HFSS software tools to find the input reflection coefficient S_{11}. The value of inductance of the via is determined in terms of S_{11} using transmission line formulation. The theoretical and experimental results for L as a function of d, h, and d/h are compared with those obtained from empirical formulae developed by the other authors. The results are found in good agreement. Secondly a square via pad is added in the trace in absence of via. The equivalent capacitance C of the pad is calculated in the same way from S_{11} as it is done for L. Finally, the PCB model is configured with a cylindrical via connected between the pad in the trace and the ground plane. The complex load impedance values are obtained from the electrical equivalent circuit of the L-C combination. This impedance is also determined from the S_{11} parameter using HFSS.

Index Terms ─ Microstrip, PCB, reflection coefficient, via, via-pad.

I. INTRODUCTION

Vias are commonly used in PCB design to interconnect traces from one layer to another layer. In high frequency region, the traces behaves as transmission lines and the via presents inductance and/or capacitance in place of a short circuit connection between the traces. The resulting discontinuity at via position produces signal reflections and problems in the return current. An equivalent inductance and capacitance of the via are evaluated by many authors [1-12] to solve the issues related to signal integrity (SI).

An empirical formula for via inductance is given by Pucel [1] considering via image in terms of physical dimensions and electrical parameters of the substrate. Goldfarb and Pucel [2] have given an empirical formulae without considering the image for cylindrical via above a ground plane. They showed that their numerical and experimental results agree well with those obtained by Hoefer and Chattopadhayay [3]. Closed-form expressions of the resistance, capacitance, and inductance for interplane 3-D vias is described by Savidis and Friedman [4]. Wu and Fan [5] investigated crosstalk among signal vias considering various geometrical parameters. Some closed form expressions for the computation of the via capacitance is developed by Ndip et al. [6]. Ndip, et al. [7] introduced layer stack up scheme to solve electromagnetic reliability problem due to return current paths through via. A physics based via model is given by Zhang and Fan [8] at low frequency depending upon the via geometry. Hernandez-Sosa and Sanchez [9] described the method for calculating the equivalent self and mutual inductance of signal vias in parallel planes. For the performance assessment and optimization of signal integrity, the closed-form expressions for the via-pad capacitance and via- inductance is presented by Isidoro-Munoz et al. [10]. The coupling of signal from the center trace to the adjacent side traces due to radiated signal from the via is analytically described by Ghosh et al. [11-12].

This paper describes the methods of finding inductance L of a cylindrical via and capacitance C due to via pad in printed circuit board from the concepts of transmission line theory and using HFSS. Initially the model of via considered is a thin cylindrical post of diameter d connected between a 50 ohm copper trace on the top of a thin FR4 - epoxy dielectric substrate and a ground plane at the bottom without considering any presence of pad on the trace. The line is terminated with matched load. The structure is simulated using HFSS to find the input reflection coefficient S_{11}. The value of inductance is determined in terms of S_{11} using transmission line formulation. The theoretical and experimental values of L versus d, h, and d/h matched well with those obtained from empirical formulae developed by the other authors ([2],[4]). Subsequently, the PCB structure is taken where a square via pad is introduced in the trace without presence of via. Since no via is connected, the equivalent circuit of the via pad

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is a capacitance C. This capacitance is calculated in the same way as it is done for L. Finally, the PCB model with a cylindrical via and a square pad is taken and the electrical equivalent impedance Z_L of the combination is determined from these L and C values. This impedance is also computed from the S_{11} parameter obtained using HFSS. The method described here introduces a good concept of finding via discontinuity impedance for academic interest.

II. TRANSMISSION LINE MODEL AND HFSS ANALYSIS

A. Inductance of via without viapad

The PCB structure considered here consists of a 50 ohm trace of length ℓ on the top of the FR4 dielectric substrate having $\varepsilon_r = 4.4$, $\tan\delta = 0.02$ and thickness h=1.6mm above a ground plane. The trace is terminated with matched loads. A cylindrical via is placed at the center of the length of the trace and connected to the ground as shown in Fig. 1. In this model it is assumed that the via diameter d<<effective wavelength λ_e inside the dielectric substrate and h<< λ_e. Since no via pad is considered, the equivalent circuit of the via is an inductance L as shown in Fig. 2. In the frequency range from 0.5GHz to 1.5GHz, the attenuation constant α due to copper and dielectric loss varies from 0.2 to 0.6nep/m and phase constant β varies from 19 to 57.4rad/m. Hence α << β and is neglected in the theory.

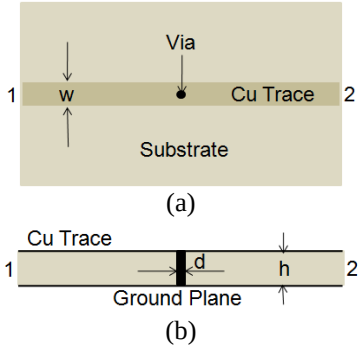


Fig. 1. Top and side view of PCB structure.

The input impedance at via position looking towards the load is given by:

$$Z_{in1} = Z_0 = 50 \text{ ohm.} \tag{1}$$

Therefore, the resultant load across via is:

$$Z_{L1} = \frac{50 \times j\omega L}{j\omega L + 50}, \tag{2}$$

which leads to:

$$L = \frac{50 Z_{L1}}{j\omega(50 - Z_{L1})}. \tag{3}$$

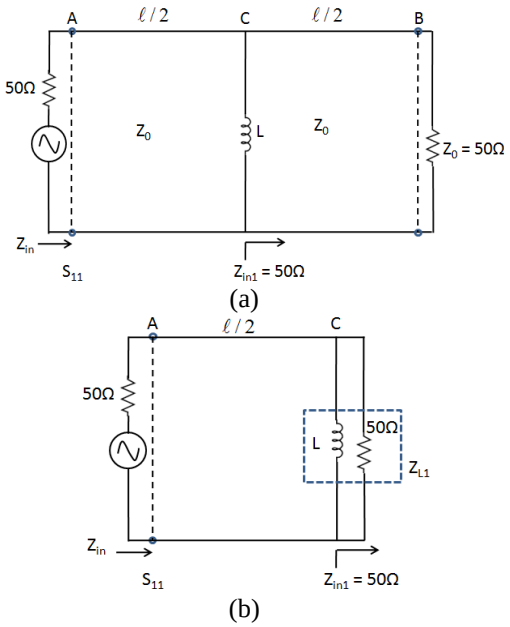


Fig. 2. Equivalent circuit.

Therefore, at the excitation port the input impedance is expressed by:

$$\frac{Z_{in}}{Z_0} = \frac{Z_{L1} + jZ_0 \tan(\beta\ell/2)}{Z_0 + jZ_{L1}\tan(\beta\ell/2)}. \tag{4}$$

Here $\beta = \frac{2\pi}{\lambda_e}$, $\lambda_e = \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}}$, and is given by [13]:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{12h}{w}\right)^{-\frac{1}{2}} \text{ ; for } \frac{w}{h} \rangle\rangle 1.$$

From equation 4 the effective load at via can be obtained as:

$$Z_{L1} = \frac{Z_{in} - jZ_0 \tan(\beta\ell/2)}{1 - j\frac{Z_{in}}{Z_0}\tan(\beta\ell/2)}. \tag{5}$$

In terms of input reflection parameter S_{11}:

$$\frac{Z_{in}}{Z_0} = \frac{1 + S_{11}}{1 - S_{11}}. \tag{6}$$

Substituting equation (6) in equation (5), and using equation (3), the via inductance can be calculated. The complex value of S_{11} is determined using simulation with HFSS and for a given value of d/h ratio via inductance L is obtained from equations (3-6).

For the similar via model, [1] has given an empirical formula for inductance considering the image concepts:

$$L = \frac{\mu_0}{4\pi}\left[2h.\ln\left(\frac{2h + \sqrt{(d/2)^2 + (2h)^2}}{d/2}\right) + \left(d/2 - \sqrt{(d/2)^2 + (2h)^2}\right)\right]. \tag{7}$$

The results of the values of L versus d, h, and d/h are described in Section III.

B. Capacitance of via pad without via

The PCB structure considered here consists of same configuration as previously taken where a square via pad is placed at the center of the length of the trace without via as shown in Fig. 3. Since no via is present, the equivalent circuit of the via pad is a capacitance as shown in Fig. 4.

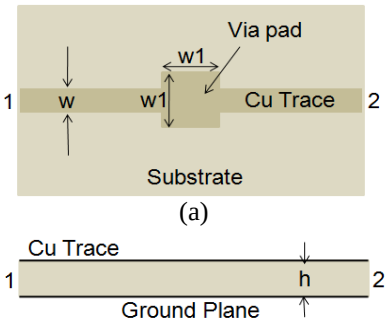


Fig. 3. Top and side view of PCB structure.

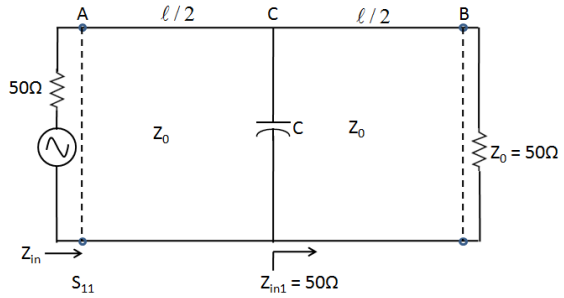
Similarly using equation (1), the resultant load across via from equivalent circuit as shown in Fig. 4 is:

$$Z_{L2} = \frac{50 \times \frac{1}{j\omega C}}{50 + \frac{1}{j\omega C}}, \tag{8}$$

which leads to:

$$C = \frac{1}{j\omega Z_{L2} 50}(50 - Z_{L2}). \tag{9}$$

The complex values of S_{11} for a different square via pad sizes (3.2, 4.2, 5.2, 6.2mm) are determined using simulation with HFSS. These values of S_{11} are used to determine Z_{L2} in the same manner as it was done for via inductance through equations (5) and (6). The capacitance C of via pad is then obtained from equation (9). The results of C versus normalized size of via pad with respect to trace width are described in Section III.



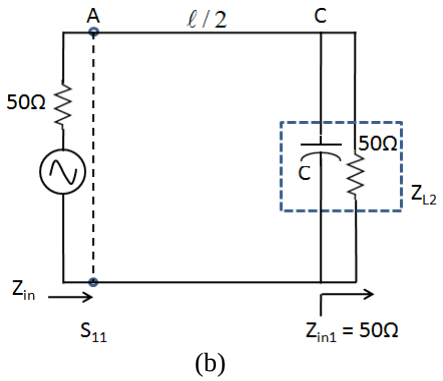


Fig. 4. Equivalent circuit.

C. Via with viapad

The PCB structure considered here consists of a cylindrical via connected to the trace through a viapad at the center of the length of the trace as shown in Fig. 5. Other end of via is connected to the ground.

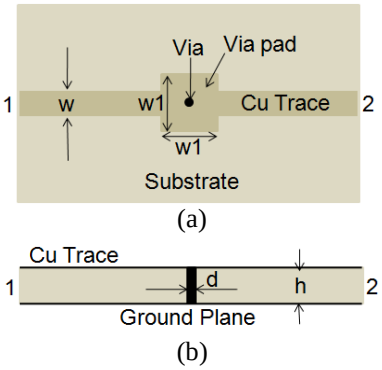


Fig. 5. Top and side view of PCB structure.

The equivalent circuit of this configuration is shown in Fig. 6. The resultant load at the via position is given by:

$$Z_{L3} = \frac{50 \times j\omega L}{50 + j\omega L - 50\omega^2 LC}. \tag{10}$$

The load impedance Z_{L3} is obtained from equation (10), by substituting the values of via inductance L (Eqn. 3) and via pad capacitance C (Eqn. 9).

In order to validate the values of L and C obtained above, the total load impedance (Fig. 6) is also computed using HFSS tool simulating the actual configuration of Fig. 5. This value is designated as Z_{Lhfss}. In the later method the complex value of S_{11} is determined to find the equivalent load impedance Z_{Lhfss} of via with via pad shunted by 50 ohm load in the similar way as it was done for via inductance through equations (5) and (6). Both the results of Z_{L3} and Z_{Lhfss} are agreed well as shown in Fig. 7 (a) and the effective impedance Z_L of the via with pad is determined from the average value

of Z_{L3} and Z_{Lhfss}.

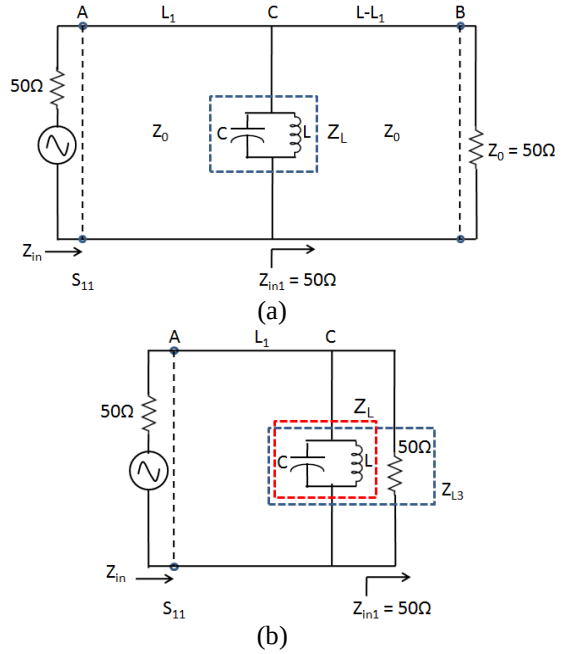


Fig. 6. Equivalent circuit.

III. RESULTS AND DISCUSSION

The geometric layout considered here consists of a 50 ohm trace of length ℓ on the top of the FR4 dielectric substrate is terminated with matched loads. The operating frequency range considered here is 0.5-1.5GHz. In the first model, since no via pad is considered, electrical equivalent parameter of via is an inductance. The inductance of cylindrical via is obtained from the concepts of transmission line theory and using HFSS. The inductance value is calculated from the input reflection coefficient. The results obtained by the present method are compared with those of [1] and experimental results as shown in Fig. 7 (b). It is found that the inductance value obtained by the present authors from equations (3-6) using transmission line theory and HFSS analysis, matched well with the results of [1] as well as of experimentation.

Analysis is further extended to find via inductance L versus d for given values of h and also L versus h for given values of d. The results are shown in Figs. 8 and 9. It is seen that the results of analytical method using transmission line theory and HFSS analysis of the present authors agree well with those of [1]. Because of limitations in fabrication facility and non-availability of substrates of different thicknesses, experimental results for very thin via and multiple thickness of substrate are not shown in Figs. 7, 8 and 9.

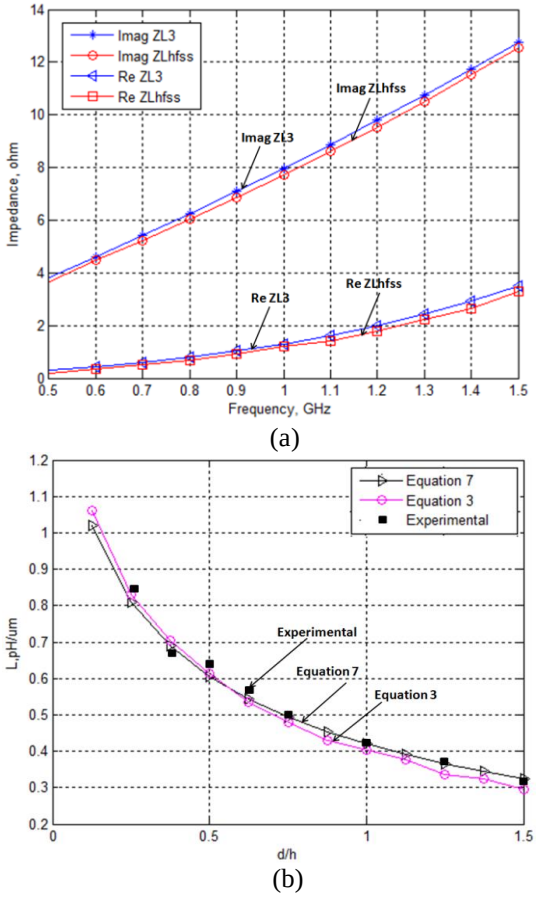


Fig. 7. (a) Input impedance versus frequency for loading with via along with pad. (b) Via inductance per unit length versus *d*/*h*.

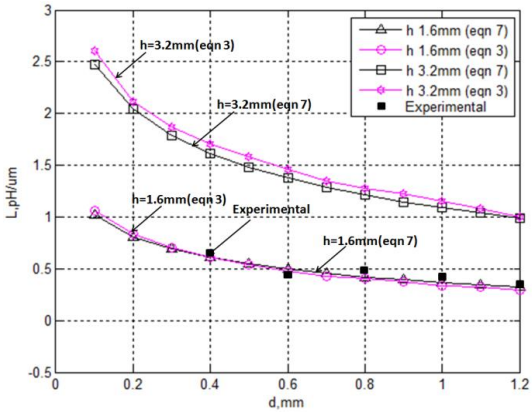


Fig. 8. Via inductance per unit length versus d for equations (9), (8), (7), and (9) with h as parameter.

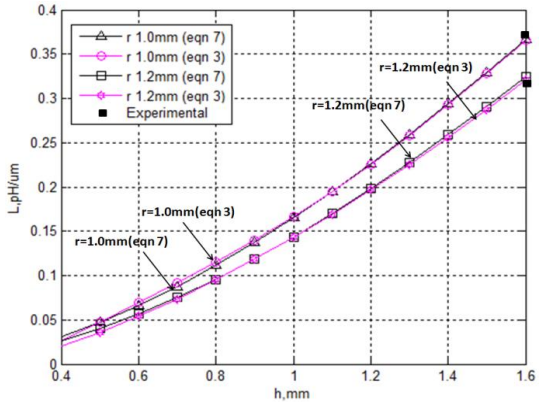


Fig. 9. Via inductance per unit length versus h for equations (9), (8), (7), and (9) with d as parameter.

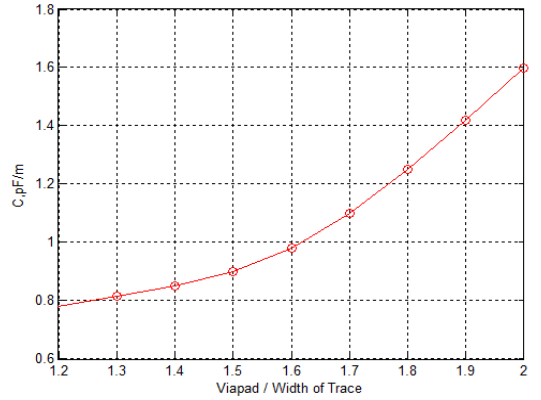


Fig. 10. Via pad capacitance per unit length versus via pad/width of trace.

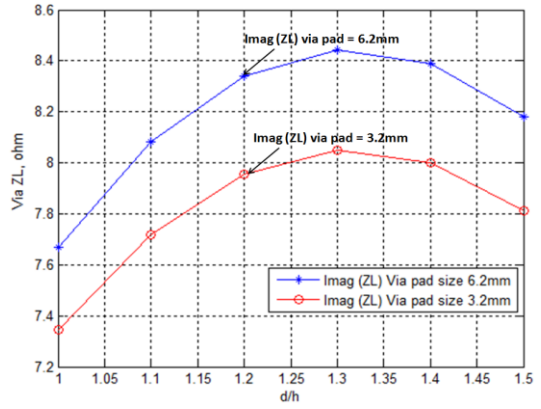


Fig. 11. Via $Z_L = R_L + jX_L$ versus d/h with via pad size as parameter.

In the second structure, electrical equivalent parameter of pad used for interfacing two layers through via is determined. The pad on a trace represents a capacitance. In this analysis this capacitance is obtained from the concepts of transmission line theory and using HFSS. The capacitance value is calculated from the input reflection coefficient. Capacitance of different sizes of the pad is determined as shown in Fig. 10. It is observed that the value of capacitance increases with increase in the size of via pad.

The Figs. 11-14 show the variation of complex impedance Z_{L3} represented by via along with pad versus d/h, pad size, and frequency.

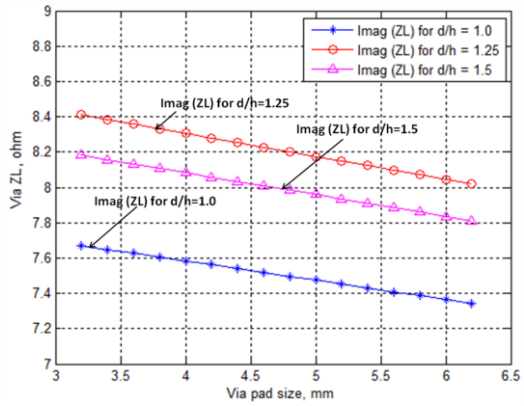


Fig. 12. Via $Z_L = R_L + jX_L$ versus via pad size with d/h as parameter.

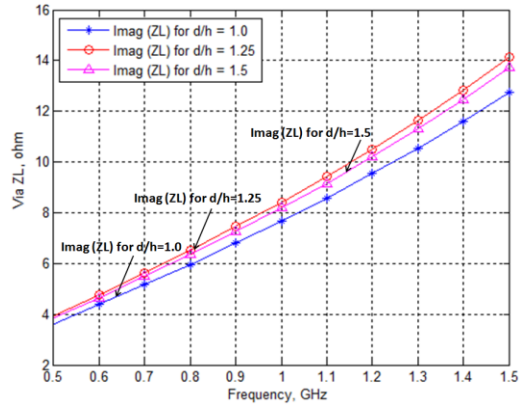


Fig. 13. Via $Z_L = R_L + jX_L$ versus frequency with d/h as parameter.

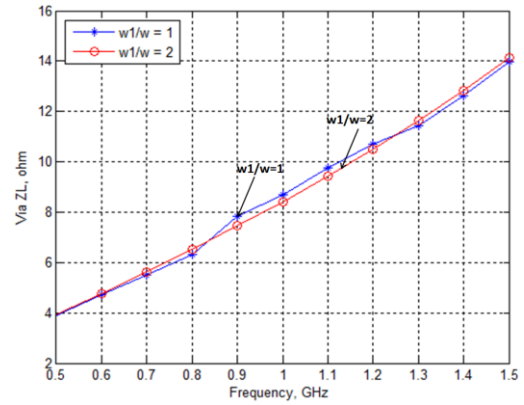


Fig. 14. Via Z_L versus frequency with normalized pad size $w1/w$ as parameter.

IV. CONCLUSION

In this paper, the methods of finding via inductance L and capacitance C of via pad in the PCB are described using transmission line theory and HFSS analysis. The theoretical and experimental results are compared with those obtained from empirical formulae developed by the other authors and found good agreement. Different PCB configurations: (a) only via without pad, (b) only via pad in absence of via, and (c) via with pad, are simulated using HFSS to find the input reflection coefficient S_{11}. The values of inductance and capacitance are determined from the complex S_{11} parameter using transmission line formulation. These values L and C are used to determine the complex load impedance Z_{L3} at via location. The model with via and its pad is simulated with HFSS. S_{11} value of this combination is determined to find the complex load impedance Z_{Lhfss} at via location. Both the results Z_{L3} and Z_{Lhfss} are compared and found good agreement.

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REFERENCES

[1] W. Hoefer and A. Chattopadhyay, "Evaluation of equivalent circuit parameters of microstrip discontinuities through perturbation of a resonant ring," *IEEE Trans. MTT*., vol. MTT-23, no. 12, pp 1067-1071, Dec. 1975.

[2] I. Savidis and E. G. Friedman, "Closed-form expressions of 3-D via esistance, inductance, and capacitance," *IEEE Transactions on Electron Devices*, vol. 56, no. 9, Sep. 2009.

[3] S. Wu and J. Fan, "Investigation of crosstalk among vias," *IEEE International Symposium on Electromagnetic Compatibility*, 2009.

[4] I. Ndip, F. Ohnimus, K. Lobbicke, C. Tschoban, M. Bierwirth, and S. Guttowski, "Equivalent circuit modeling of signal vias considering their return current paths," *2010 Asia Pacific International Symposium on Electromagnetic Compatibility*, Beijing, China, Apr. 12-16, 2010.

[5] I. Ndip, F. Ohnimus, S. Guttowski, and H. Reichl, "Modeling and analysis of return-current paths for microstrip-to-microstrip via transitions," *IEEE Electronic System-Integration Technology Conference(ESTC 2008)*, London, UK, Sep. 1-4, 2008.

[6] Y. Zhang and J. Fan, "Recent development of via models: Hybrid circuit and field analysis," *IEEE Electr. Design Adv. Package. Syst. Symp*., Dec 2010.

[7] G. Hernandez-Sosa and A. Sanchez, "Analytical calculation of the equivalent inductance for signal vias in parallel planes with arbitrary P/G via distribution," *8th International Caribbean Conference on Devices, Circuts and Systems (ICCDCS)*, 2012.

[8] A. Isidoro-Munoz, R. Torres-Torres, M. A. Tlaxcalteco-Matus, and G. Hernandez-Sosa, "Scalable models to represent the via-pad capacitance and via-traces inductance in multilayer PCB high speed interconnects," *International Conference on Devices, Circuits and Systems (ICCDCS)*, 2017.

[9] A. Ghosh, S. K. Das, and A. Das, "Analysis of radiation coupling from via in multilayer printed circuit board traces," *14th International Conference on Electromagnetic Interference & Compatibility (INCEMIC 2016)*, Bengaluru, India, Dec. 8-9, 2016.

[10] A. Ghosh, S. K. Das, and A. Das, "Analysis of crosstalk in high frequency printed circuit boards in presence of via," *International Conference on Electromagnetics in Advanced Applications IEEE-APS Topical Conference on Antennas and Propagation in Wireless Communications 2017*, Verona, Italy, Sep. 11-15, 2017.

[11] E. O. Hammerstad, "Equations for microstrip circuit design," *5th European Microwave Conference*, 268, 1975.

[12] Ansoft High Frequency Structure Simulation (HFSS), ver. 10, Ansoft Corporation, Pittsburgh, PA, 2005.