Fault Current Study of Inverter Interfaced Distributed Generators

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ABSTRACT

The fault current characteristics of inverter interfaced distributed generators (IIDGs) are very different from those of traditional synchronous generator. Prior to the fault current analysis of IIDG, a control strategy for low voltage ride-through (LVRT) of IIDG is proposed to meet the grid code. Then the fault current characteristics of IIDG are analyzed based on the study of dynamic responses of the inverter under conditions of symmetric faults and asymmetric faults. Meanwhile, the analytical expressions of the fault current of IIDG are obtained. Finally, the fault current characteristics of IIDG are validated with simulation studies.

Keywords: power electronics, inverter-interfaced distributed generator (IIDG), dynamic response, fault current, analytical expression

INTRODUCTION

In order to make comprehensive utilization of the renewable and environmental friendly energy sources, as well as improve the power system's capability against natural disaster, distributed generators (DGs) which include wind turbine generator system, photovoltaic generation system, fuel cell and so on have been developed and applied widely in the recent years [1], [2]. Among them, most types of DGs interface to the medium voltage or low voltage distribution network with inverters, which can be classified as inverter interfaced distributed generators (IIDGs).

Prior to the introduction of IIDGs into distribution network in large scale, the conventional distribution network in China is designed to operate radially, and the three-stage current direction insensitive

protections are adopted. However, the performance of the three-stage current protections has been greatly deteriorated by the introduction and low voltage ride-through (LVRT) of IIDGs [3, 4] from the following aspects. 1) The fault current characteristics of IIDGs are much different from those of conventional synchronous generator. 2) The power outputs of IIDGs are random and discontinuous, since they are influenced by natural environment and climate. 3) The introduction of IIDGs results in bidirectional flow of power and changes the fault current level. Hence, the increasing penetration of IIDGs to the distribution network has resulted in lots of technical challenges for the existing relaying protections [5-8].

An approach to addressing the relaying protection problems is to study the dynamic responses of IIDG under fault conditions, and then propose novel protection schemes. Scholars have carried out lots of research works in this respect. The fault characteristics of IIDG in islanded microgrid are studied in [9, 10]. However, since the control strategy of grid-connected IIDG is different from that of islanded IIDG, the fault current characteristics of grid-connected IIDG are also much different from those of islanded IIDG, which need to be studied specifically. In [11], though the fault characteristics of IIDG with P-Q control or V-f control are studied, sufficient theoretical analysis is absent. The fault characteristics of grid-connected IIDG are also studied in [12]. However, the requirement that IIDG should provide reactive power support for the power grid during fault period [3, 4] is not taken into account.

To fill this gap, with consideration of the requirement of the grid code, the fault current characteristics of IIDG are studied in this paper. Firstly, a control strategy for LVRT of IIDG is proposed. Based on it, the responses of inverter under all kinds of fault conditions are studied. Then the fault current characteristics of IIDG under various fault conditions are analyzed and the analytical expressions are obtained. Meanwhile, simulation cases are studied with PSCAD/EMTDC to validate the analytical results. Finally, the general remarks of this paper are highlighted.

CONTROL STRATEGY FOR LVRT OF IIDG

Power Decoupling Control Strategy under Steady State

The inverter of IIDG is shown in Figure 1.

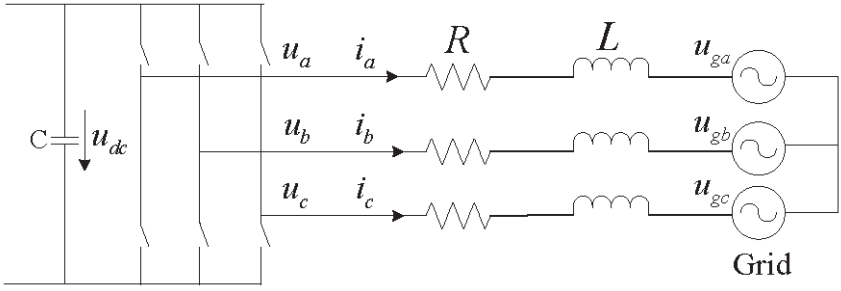

Figure 1. Inverter of IIDG

The synchronous *dq* reference frame is chosen to model the inverter of IIDG and the mathematical equations are expressed in (1).

$$\begin{cases} u_d = Lpi_d + Ri_d - \omega_1 Li_q + u_{gd} \\ u_q = Lpi_q + Ri_q + \omega_1 Li_d + u_{gq} \end{cases} \tag{1}$$

where u_d and u_q are respectively the *d*-axis and *q*-axis components of the inverter output voltage, u_{gd} and u_{gq} are respectively the *d*-axis and *q*-axis components of the grid voltage, i_d and i_q denote the *d*-axis and *q*-axis components of the inverter output current respectively, ω_1 represents the angular velocity of the reference frame, *L* is the AC filter inductance, and *R* represents the equivalent resistance of the filter inductance.

With application of PI controller and feed forward compensation, the current control equations of the inverter can be expressed in (2).

$$\begin{cases} u_d = \left(k_P + k_I / s\right)\left(i_d^* - i_d\right) + Ri_d + \omega_1 Li_q + u_{gd} \\ u_q = \left(k_P + k_I / s\right)\left(i_q^* - i_q\right) + Ri_q - \omega_1 Li_d + u_{gq} \end{cases} \tag{2}$$

where k_p and k_I are the proportional gain and integral gain of the inner current controller respectively, i_d^* and i_q^* are the reference signals of the *d*-axis and *q*-axis components of the output current respectively.

Let the *d*-axis of the reference frame is aligned with the grid voltage vector, and it can be obtained consequently that

$$u_{gd} = \left|\dot{U}_g\right| = U_g$$

$$u_{gd} = \left|\dot{U}_g\right| = U_g, \quad u_{gq} = 0 \tag{3}$$

where U_g is the magnitude of the grid voltage vector.

Hence, the output powers of the inverter are:

$$\begin{cases} P = u_{gd} i_d + u_{gq} i_q = U_g i_d \\ Q = u_{gq} i_d - u_{gd} i_q = -U_g i_q \end{cases} \tag{4}$$

From (4), it can be obtained that the active and reactive power can be decoupled and regulated respectively by the d -axis and q -axis components of the output current. Actually, the dc-link voltage is closely related to the active power. Hence, the dc-link voltage can be regulated by the control of i_d, and the power factor can be regulated by the control of i_q.

Consequently, the control diagram of IIDG as shown in Figure 2 can be obtained.

As Figure 2 shows, the control scheme based on an external power-voltage control loop and an inner current control loop is adopted.

Proposed Control Strategy for LVRT

It is known that the fault current characteristics of IIDG are predominantly influenced by the LVRT control strategy of IIDG. Hence, the control strategy for LVRT of IIDG should be taken into account. In this paper, the LVRT of IIDG will be implemented according to the grid technical guideline issued by Germany [3].

Since the inertia time constant of IIDG is very small, the LVRT of IIDG can be implemented by changing the control strategy without additional hardware devices. Consequently, the following control strategy for LVRT of IIDG is proposed, as shown in Figure 3.

(1) Due to the fault duration is normally very short and energy storage device is usually equipped with IIDG, the dc-link voltage is considered constant during grid fault. In this context, in order to improve the response speed of IIDG, the external power-voltage control loop is shut down if the positive-sequence component of the grid voltage is smaller than 0.9 p.u. Then give the reference signals directly to the inner current control loop.

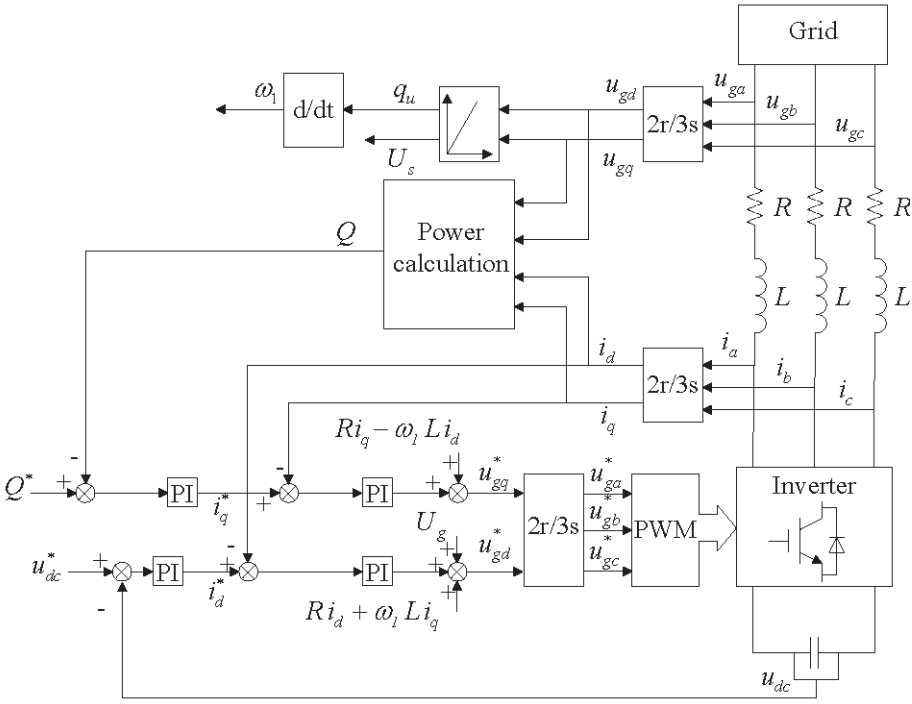

Figure 2. Control diagram of IIDG inverter

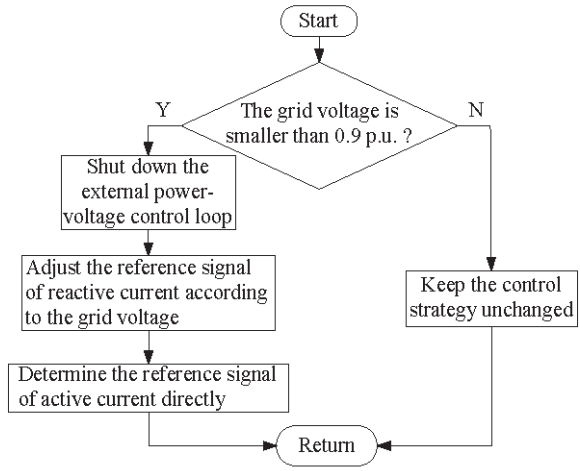

Figure 3. Flow chart of control strategy for LVRT of IIDG

(2) In order to provide sufficient reactive current to meet the requirements of the German grid code, the reactive current reference signal denoted by i_q^* during grid fault should be:

$$i_q^* = \begin{cases} 0 & \alpha > 0.9 \\ 2*(1-\alpha) & 0.4 \le \alpha \le 0.9 \\ 1.2 & \alpha < 0.4 \end{cases} \quad (5)$$

where all parameters are given in per unit system, and α represents the magnitude of the positive-sequence grid voltage after a fault occurs.

(3) Moreover, in order to ensure the safety of IIDG and at the same time do the best to keep the balance of active power, the maximum active current which is within the admissible overload capability of IIDG (the photovoltaic power station can work stably and continuously with the output current up to 1.2 p.u. more than 1 minute [3]) should also be provided. Hence, the active current reference signal denoted by i_d^* should be the smaller one of $i_{d\,0}^*$ and $\sqrt{1.2^2 - i_q^{*2}}$. $i_{d\,0}^*$ is the active current reference signal before the fault occurs.

FAULT CURRENT STUDY OF IIDG

For the following analysis, instantaneous grid voltage dip [13] is taken as an example to study the fault current characteristics of IIDG for sake of simplicity.

Fault Current Study under Conditions of Symmetric Voltage Dips

Since the external control loop is shut down during the grid fault, the block diagram of the inner current control loop is shown in Figure 4.

In Figure 4, $G_i(s) = k_P + k_I / s$ is the transfer function of PI controller. $K_{inv} / (1 + sT_p)$ is a first order inertial element representing the transfer function of the inverter. K_{inv} is the equivalent gain of the inverter, and T_P is the lagging time constant. $1/(R + sL)$ is the transfer function of the AC filter.

T_P can be neglected as it is very small, and $K_{inv} = 1$ [14]. Hence, taking the control diagram of *d*-axis component for example, the simplified control diagram is shown in Figure 5.

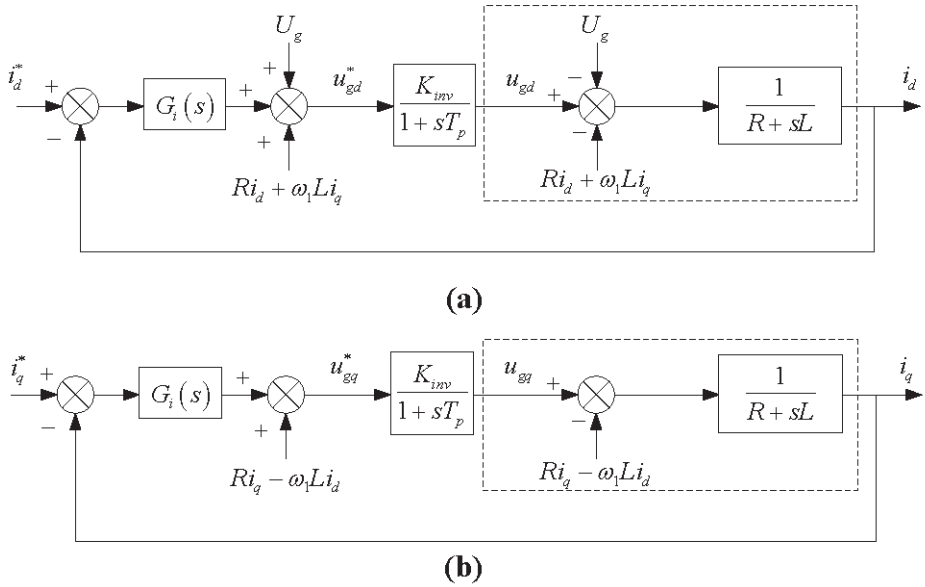

Figure 4. (a) control diagram of d-axis component, (b) control diagram of q-axis component.

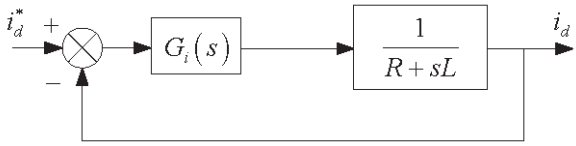

Figure 5. Simplified block diagram of d-axis component

Obtained from Figure 5, the closed-loop transfer function of the *d*-axis component of the output current is

$$G_{cl}(s) = \frac{i_d}{i_d^*} = \frac{G_i(s)}{G_i(s) + R + sL} \tag{6}$$

In order to track the reference signal quickly, it can design the inner current controller to be a typical first order system [14] which means

$$G_{cl}(s) = \frac{1}{1 + (s/\omega_c)} \tag{7}$$

where $\omega_c = 2\pi f_c$ and f_c is the desired closed-loop bandwidth of the inner current control loop. In the engineering practice, f_c should be within 1/5 of the equivalent switching frequency [14]. In this paper, the equivalent switching frequency is chosen to be 2.5 kHz. Hence, it can set ω_c to be $10\omega_1$ which makes f_c to be 1/5 of the equivalent switching frequency. Consequently,

$$k_P = \omega_c L, \quad k_I = \omega_c R \tag{8}$$

Assuming the active current reference signal before the fault occurs is i_{d0}^* and changes to be i_{d1}^* after the fault occurs, the *d*-axis component of the fault component current provided by IIDG is

$$\Delta i_{df}(s) = G_{cl}(s)[i_{d1}^*(s) - i_{d0}^*(s)] = \frac{1}{1+(s/\omega_c)} \frac{i_{d1}^* - i_{d0}^*}{s} = (i_{d1}^* - i_{d0}^*)\left(\frac{1}{s} - \frac{1}{s+\omega_c}\right) \tag{9}$$

where "Δ" indicates fault component.

Applying inverse Laplace transformation to (9), the following expression can be obtained.

$$\Delta i_{df}(t) = (i_{d1}^* - i_{d0}^*)(1 - e^{-\omega_c t}) \tag{10}$$

Since the damping time constant $\tau = 1/\omega_c \approx 0.32$ ms. It means that the transient period of $\Delta i_{df}(t)$ is approximately 1.0 ms which can be neglected. As a result, it can be approximately considered that

$$\Delta i_{df}(t) \approx i_{d1}^* - i_{d0}^* \tag{11}$$

Likewise, the obtained expression of the *q*-axis component of the fault component current is

$$\Delta i_{qf}(t) \approx i_{q1}^* - i_{q0}^* \tag{12}$$

where i_{q0}^* is the reactive current reference signal before the fault occurs, and i_{q1}^* is the reactive current reference signal after the fault occurs.

Since IIDG is under steady state and operates with unity power

factor before the fault occurs,

$$i_{d0}(t) = i_{d0}^{*}, \quad i_{q0}(t) = 0 \tag{13}$$

Consequently, the three-phase currents of IIDG before the fault occurs are

$$\begin{cases} i_{sa0}(t) = i_{d0}^{*} \cos(\omega_1 t + \theta_i) \\ i_{sb0}(t) = i_{d0}^{*} \cos(\omega_1 t + \theta_i - 2\pi/3) \\ i_{sc0}(t) = i_{d0}^{*} \cos(\omega_1 t + \theta_i + 2\pi/3) \end{cases} \tag{14}$$

where θ_i is the initial phase angle of the Phase A current.

The *d*-axis and *q*-axis components of the fault current provided by IIDG after the fault occurs are

$$\begin{cases} i_{d1}(t) = i_{d0}(t) + \Delta i_{df}(t) = i_{d1}^{*} \\ i_{q1}(t) = i_{q0}(t) + \Delta i_{qf}(t) = i_{q1}^{*} \end{cases} \tag{15}$$

Hence, the three-phase currents of IIDG after the fault occurs are

$$\begin{cases} i_{sa1}(t) = \sqrt{i_{d1}^{*2} + i_{q1}^{*2}} \cos(\omega_1 t + \theta_i + \varphi) \\ i_{sb1}(t) = \sqrt{i_{d1}^{*2} + i_{q1}^{*2}} \cos(\omega_1 t + \theta_i - 2\pi/3 + \varphi) \\ i_{sc1}(t) = \sqrt{i_{d1}^{*2} + i_{q1}^{*2}} \cos(\omega_1 t + \theta_i + 2\pi/3 + \varphi) \end{cases} \tag{16}$$

where $\varphi = \arctan(i_q^{*}{}_1 / i_d^{*}{}_1)$.

It can be obtained from (16) that the fault current characteristics of IIDG are different from those of conventional synchronous generator. Since IIDG interface to the power grid with inverter, the inertia time constant is very small. Hence, the transient component of the fault current provided by IIDG can be neglected. It can be approximately considered that IIDG transfers to the steady-state operating condition directly, without damped dc component and damped fundamental frequency component in the output current of IIDG.

With comparison between (14) and (16), both the magnitude and phase angle of the output current of IIDG change due to the fault occurrence. The change amounts of the magnitude and phase angle is related to the operating condition of IIDG before the fault occurs and the grid voltage after the fault occurs.

Fault Current Study under Conditions of Asymmetric Voltage Dips

For asymmetrical voltage dips, the adequate phase-locked loop [15] can help to identify the phase angle and magnitude of the positive-sequence voltage quickly and accurately. Hence, the active and reactive current reference signals after the fault occurs can be obtained according to (5).

With the regulation of the PI controller of the inner current control loop, the *d*-axis and *q*-axis components of the output current of IIDG can track the corresponding reference signals so quickly that the transient period can be neglected. Since only the positive-sequence voltage is used to generate the current reference signals, there is also only the positive-sequence component in the fault current provided by IIDG under conditions of asymmetrical voltage dips. Meanwhile, the expressions of the output current are the same with (15). Hence, it can be found that the fault current characteristics of IIDG under conditions of asymmetrical voltage dips are much different from those of conventional synchronous generator.

Besides, the magnitude and phase angle of the fault current are also related to the operating condition of IIDG before the fault occurs and the positive-sequence grid voltage after the fault occurs.

CASE STUDY

In order to validate the above analysis results, simulation model with IIDG is built with PSCAD/EMTDC. The parameters of IIDG are given as follows.

Rated capacity: 10.0 MVA
Rated voltage: 10.5 kV
AC filter inductance: 0.1 mH
Equivalent resistance of the AC filter: 1.0 mΩ

For the following case study, it is noted that i_{rd} and i_{rq} are respectively the simulation results of the *d*-axis and *q*-axis components of the

output current of IIDG; i_{rdref} and i_{rqref} represent the active and the reactive current reference signals. Meanwhile, according to (15), i_{rdref} and i_{rqref} are also the theoretical analysis results of the *d*-axis and *q*-axis components of the output current of IIDG respectively.

Case Study under Condition of Symmetric Voltage Dip

The fault condition where a symmetrical grid voltage dip down to 0.4 p.u. occurs at t=1.0s is taken as an example.

On condition that IIDG is fully loaded before the fault occurs, Figure 6 depicts the comparison between the theoretical analysis results and simulation results of the *d*-axis and *q*-axis components of the output current provided by IIDG. Moreover, Figure 7 shows the fault current of Phase A i_a, its magnitude i_{am} and phase difference between the current and voltage P_{ui}.

According to the proposed control strategy for LVRT, i_{rqref} is 1.2 p.u. and i_{rdref} is zero after the fault occurs, as shown in Figure 6. Meanwhile, it can be found that i_{rd} and i_{rq} can track i_{rdref} and i_{rqref} very quickly. The error between i_{rd} and i_{rdref} and the error between i_{rq} and i_{rqref} are both within ±0.05, which validates the theoretical analysis results of the fault current characteristics of IIDG. Besides, the sufficient reactive power and maximum possible active power can be provided by IIDG to offer network support throughout the grid voltage dips.

As Figure 7 shows, the magnitude of the output current changes from 1.0 p.u. to 1.2 p.u., and the phase difference between the current and voltage changes from 0° to 90°.

On condition that IIDG is unloaded before the fault occurs, Figure 8 elaborates the comparison between the theoretical analysis results and simulation results of the *d*-axis and *q*-axis components of the output current provided by IIDG. Moreover, Figure 9 shows the fault current of Phase A i_a, as well as its magnitude i_{am}. The phase difference between the current and voltage is not given here, since the output current of IIDG is zero before the fault occurs and the phase difference is meaningless.

As shown in Figure 8, with the proposed control strategy for LVRT, i_{rqref} is 1.2 p.u. and t i_{rdref} is zero after the fault occurs. It can be also observed that i_{rd} and i_{rq} can track i_{rdref} and i_{rqref} very quickly. The error between i_{rd} and i_{rdref} and the error between i_{rq} and i_{rqref} are both within ±0.05. In this context, the theoretical analysis results of the fault current characteristics of IIDG are validated, and the sufficient reactive power can be provided.

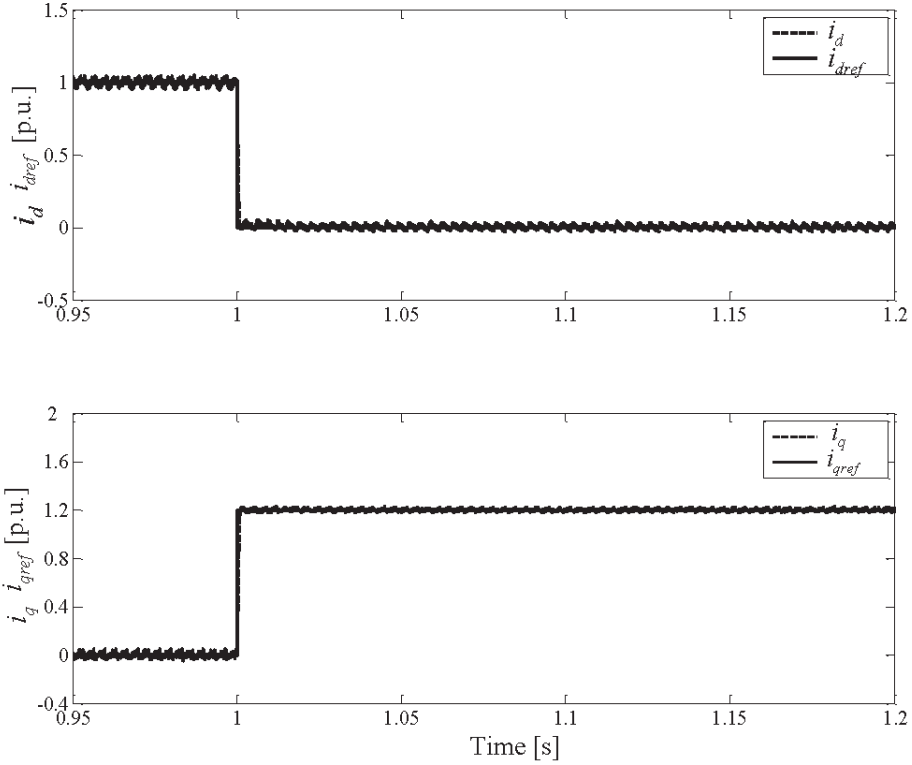

Figure 6. d-axis and q-axis components of the fault currents on condition that IIDG is fully loaded before the fault occurs

As Figure 9 shows, the magnitude of the output current of IIDG changes from zero to 1.2 p.u.

Case Study under Condition of Asymmetric Voltage Dip

The fault condition where both the voltage magnitudes of Phase B and Phase C drop from 1.0 p.u. to 0.4 p.u. at t=1.0s is taken as an example.

On condition that IIDG is fully loaded before the fault occurs, Figure 10 depicts the comparison between the theoretical analysis results and simulation results of the d-axis and q-axis components of the output current provided by IIDG. Moreover, Figure 11 demonstrates the three-phase currents i_{abc}, fault current magnitude of Phase A i_{am}, and phase difference between the current and positive-sequence voltage of Phase A P_{ui}.

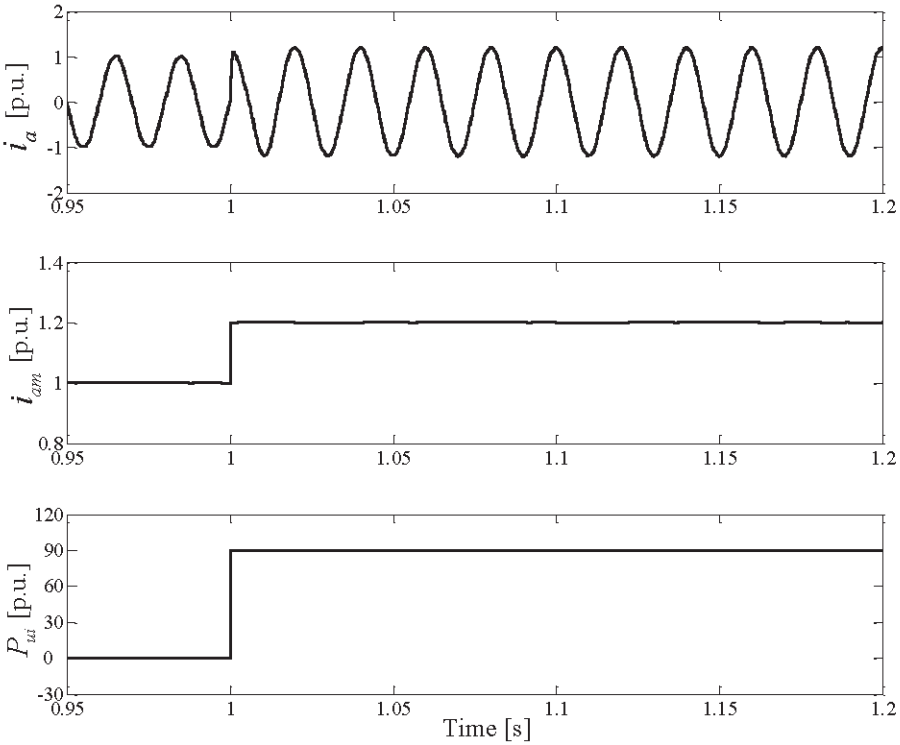

Figure 7. Fault current of Phase A on condition that IIDG is fully loaded before the fault occurs

Since both the voltage magnitudes of Phase B and Phase C drop from 1.0 p.u. to 0.4 p.u., the magnitude of the positive-sequence grid voltage change from 1.0 p.u. to approximately 0.6 p.u. Hence, according to the proposed control strategy for LVRT, i_{rqref} is 0.8 p.u. and i_{rdref} is 0.89 p.u. after the fault occurs, as shown in Figure 10.

Meanwhile, it can be seen from the Figure 10 that t i_{rd} and i_{rq} can track i_{rdref} and i_{rqref} very quickly. The error between i_{rd} and i_{rdref} and the error between i_{rq} and i_{rqref} are both within ±0.05. In this context, not only the sufficient reactive power and maximum possible active power are provided by IIDG to offer network support throughout the grid voltage dips, but also the theoretical analysis results of the fault current characteristics of IIDG are validated.

As shown in Figure 11, although the unbalanced grid voltage dip occurs, there is only positive-sequence component in the output current

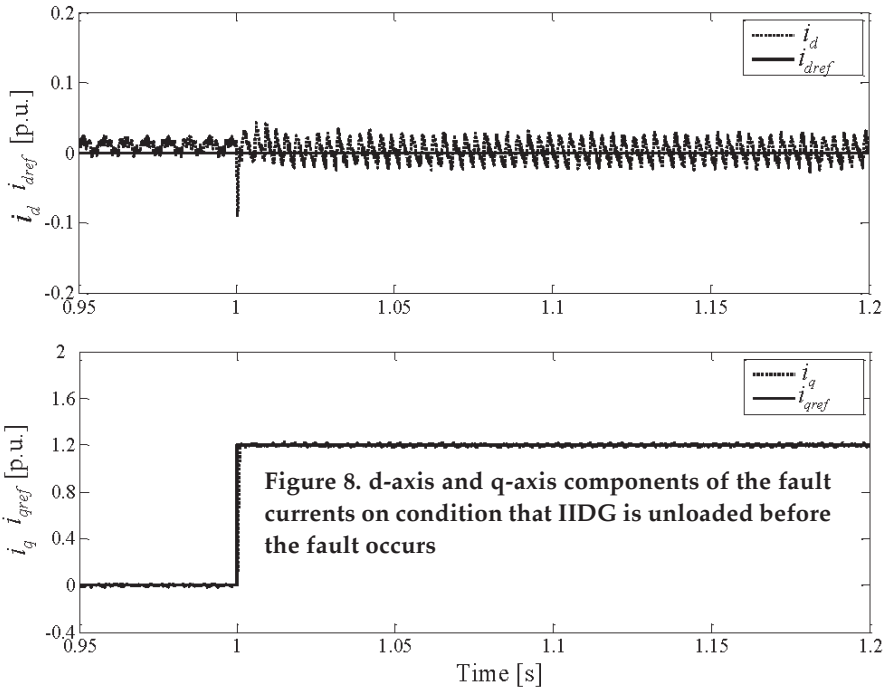

Figure 8. d-axis and q-axis components of the fault currents on condition that IIDG is unloaded before the fault occurs

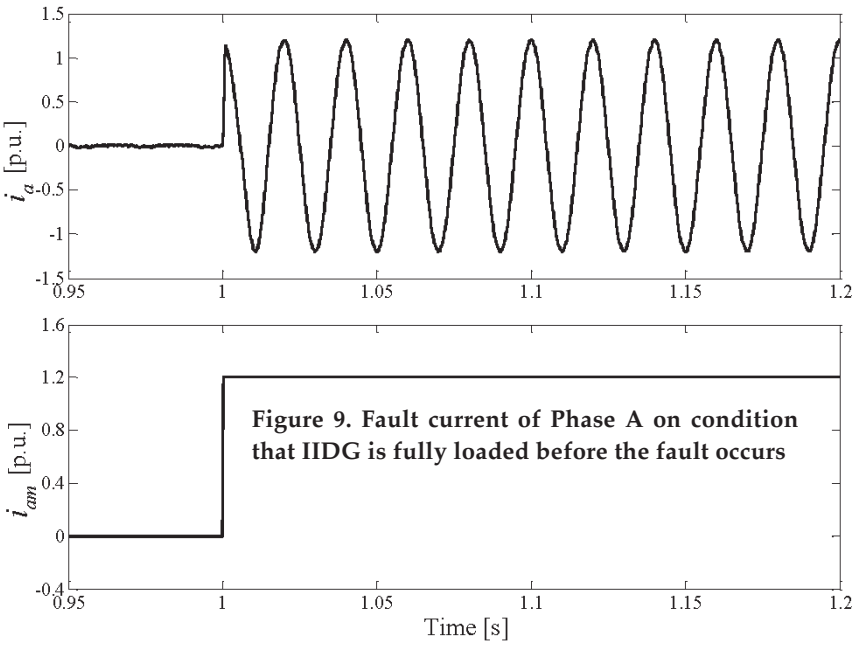

Figure 9. Fault current of Phase A on condition that IIDG is fully loaded before the fault occurs

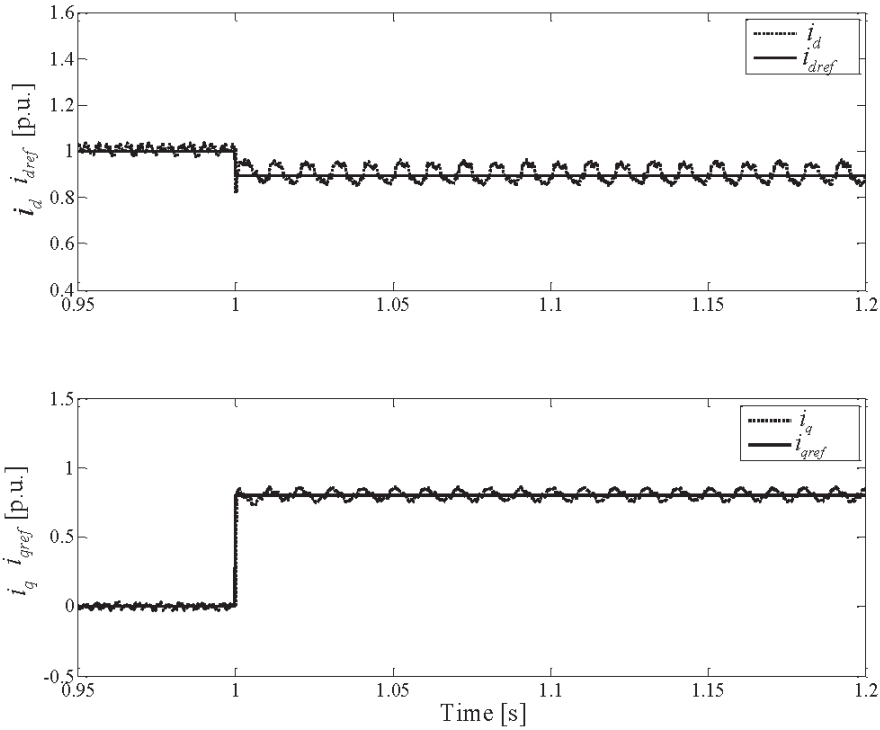

Figure 10. d-axis and q-axis components of the fault currents on condition that IIDG is fully loaded before the fault occurs

of IIDG. Besides, the magnitude of the output current changes from 1.0 p.u. to 1.2 p.u., and the phase difference between the current and positive-sequence voltage of Phase A changes from 0° to 42.4°.

On condition that IIDG is unloaded before the fault occurs, Figure 12 elaborates the comparison between the theoretical analysis results and simulation results of the *d*-axis and *q*-axis components of the output current provided by IIDG. Moreover, Figure 13 illustrates the three-phase currents i_{abc} and fault current magnitude of Phase A i_{am}.

As shown in Figure 12, according to the proposed control strategy for LVRT, i_{rqref} is 0.8 p.u. and i_{rdref} is still zero after the fault occurs. It can also be seen that i_{rd} and i_{rq} can track i_{rdref} and i_{rqref} very quickly with the control of the inverter. The error between i_{rd} and i_{rdref} and the error between i_{rq} and i_{rqref} are both within ±0.05. Hence, both the enhanced LVRT capability of IIDG and the theoretical analysis results of the fault current characteristics of IIDG are validated.

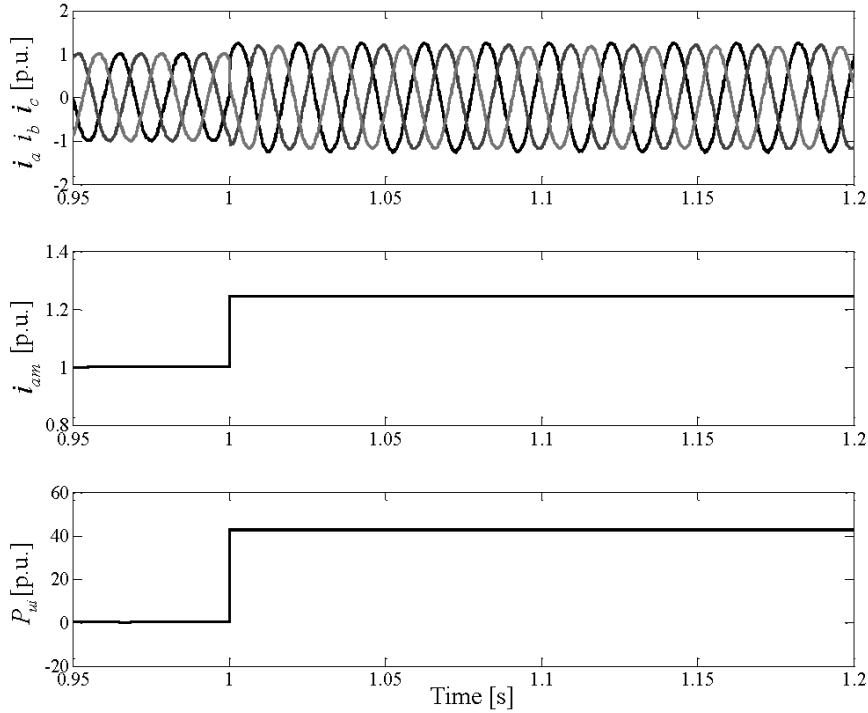

Figure 11. The three-phase currents on condition that IIDG is fully loaded before the fault occurs

As Figure 13 shows, there is only positive-sequence component in the output current of IIDG and the magnitude of the output current changes from zero to 0.8 p.u.

VERIFICATION AND VALIDATION OF THE SIMULATION MODEL

Since there is no existing simulation model which can be used to realize the proposed control strategy for LVRT of IIDG, the PSCAD/EMTDC software environment is adopted to build the required simulation model.

The simulation model is built according to Figure 2 and Figure 3. In this context, the mathematic equations and logic of the simulation model are verified. Moreover, in the simulation model, the grid is repre-

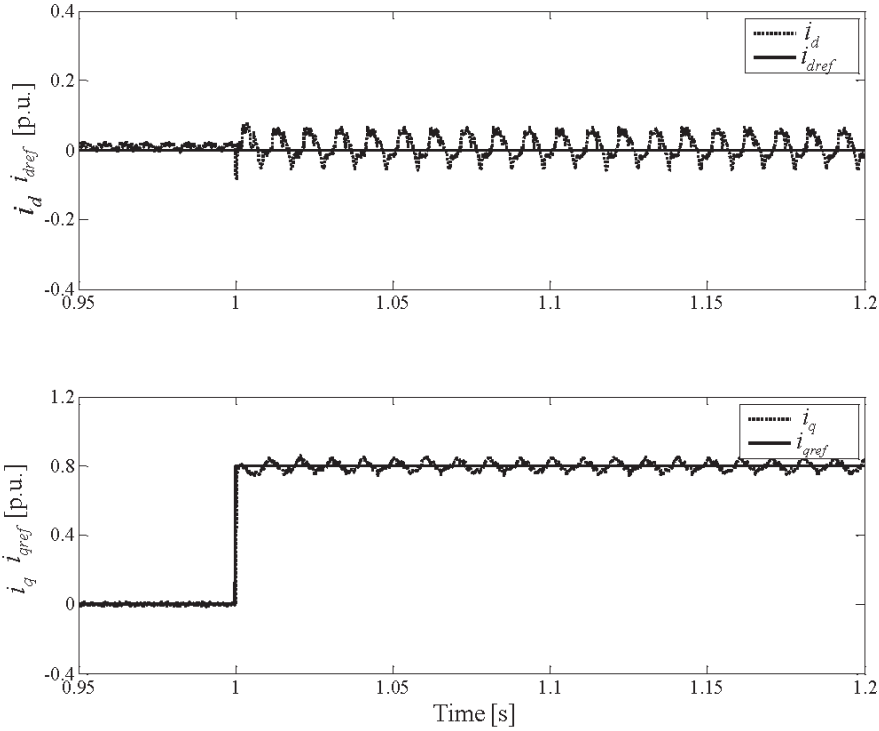

Figure 12. d-axis and q-axis components of the fault currents on condition that IIDG is unloaded before the fault occurs

sented by an ideal voltage source, and the AC filter is represented by a branch which consists of a resistor and an inductor. Besides, triangular wave signal generator and comparator are used to generate the PWM signals for the power electronic switches. Generally speaking, the simulation model consists of basic modules (such as resistor, inductor, signal generator, comparator, PI controller and so on) which are provided by PSCAD/EMTDC and have been validated by lots of users all over the world for many years. It means that the simulation model is technically correct. Furthermore, according to Figure 6, Figure 8, Figure 10 and Figure 12, the simulation results agree with the theoretical analysis results quite well, since the errors between the simulation results and the theoretical analysis results are within ±0.05. Hence, the simulation results and the theoretical analysis results can verify each other.

Besides, both in the simulation model and theoretical analysis, the dc-link voltage is considered constant during grid fault. With the fast

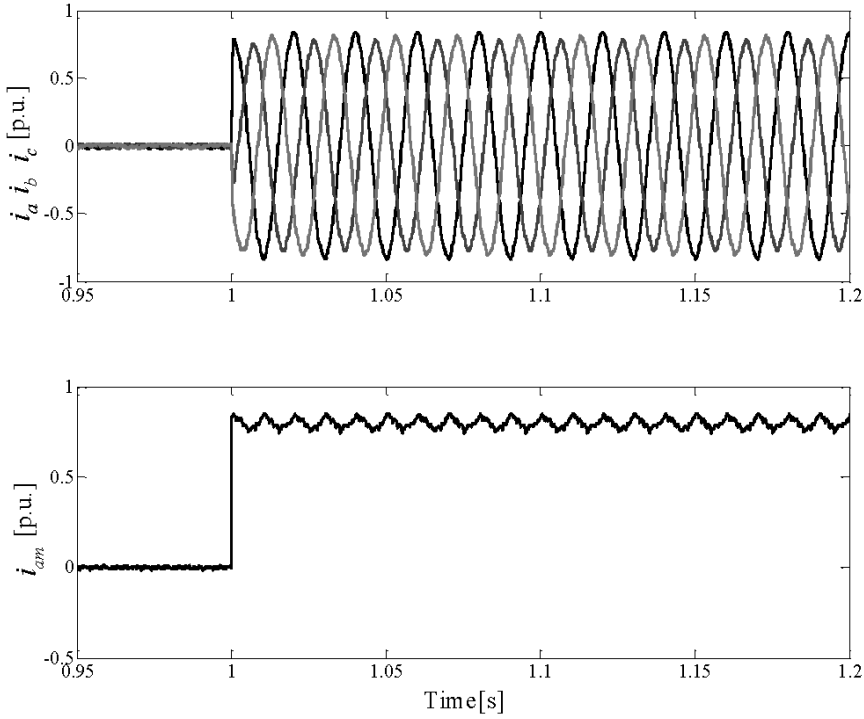

Figure 13. The three-phase currents on condition that IIDG is unloaded before the fault occurs

development of energy storage technologies, the energy storage systems are very promising for improving power quality, enhancing LVRT ability and smoothing the power fluctuation. Moreover, complementing DGs with energy storage systems has been reported in various cases [16-20]. As stated in [17], the rated value of the dc-link voltage is 1200V, and the fluctuation range of the dc-link voltage can be limited to ±50 V with the integration of the energy storage system. Hence, with the integration of the energy storage system, the dc-link voltage fluctuation during grid fault can be limited to a very small range (±5%) during grid fault. In this context, the above assumption can be valid on condition that the energy storage system is adopted.

Due to the dc-link voltage fluctuation, there will be harmonics in the fault current provided by IIDG in the realistic system. However, since the dc-link voltage fluctuation is limited to ±5%, the harmonic currents should be also very small and limited to ±5%. It means that the

discrepancies of the simulation model outputs with the actual results are limited to ±5%. Hence, discrepancies are so small and can be neglected.

CONCLUSION

In order to meet the reactive power support requirement of grid code, a control strategy for low voltage ride-through of IIDG is proposed in this paper. Based on it, the fault current characteristics of IIDG under conditions of symmetrical faults and asymmetrical faults are studied. The obtained conclusions can be drawn as follows.

1) With the proposed control strategy for low voltage ride-through, the sufficient reactive power and maximum possible active power can be provided by IIDG to offer network support throughout the grid voltage dips.

2) The fault current characteristics of IIDG are much different from those of conventional synchronous generator. No matter under conditions of symmetrical faults or asymmetrical faults, there is only the positive-sequence current provided by IIDG.

3) Since IIDG interface to the power grid with inverter, the inertia time constant is very small. Hence, it can be approximately considered that there is no damped dc component and damped fundamental frequency component in the output current of IIDG.

The research results are helpful to the LVRT capability improvement of IIDG and of great significance for the study of adequate relaying protection for the power grid with penetration of IIDGs.

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