Dead-Time Effect and Compensation Technology for an Isolated Dual Active Bridge Converter

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Abstract

Aiming at deficiencies of output voltage distortion and circulating current generation caused by dead-time effect in the modulation process, a simple and feasible dead time compensation strategy is presented. Firstly, the influence of dead-time effect on the output voltage of bridge is analysed, and a dead time compensation strategy is added between the modulation signal and dead time procession. According to the current direction of the bridge, the rising edge or falling edge of the driving signal is selectively delayed to compensate for dead-time effect. Secondly, an Optimized Triple Phase-shift (OTPS) modulation strategy is adopted with minimizing leakage inductor current Root-Mean-Square (RMS) control, which minimizes current stress, achieves soft-switching operation, avoids phase-shift errors caused by

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Dead-Time Effect, and optimizes control performance of DC-DC converters. Finally, simulated and experimental results are added to verify the correctness and effectiveness of the proposed method.

Keywords: Dead-time effect, dead time compensation technology, dual active bridge converter, minimum current stress, triple phase-shift (TPS).

1 Introduction

With the fact of fossil energy exhaustion and global ecology environment deterioration, renewable energy generation has become one of the major development trends of the modern power systems. Therefore, the key equipment of renewable energy systems has also become research hotspot [1–5]. As one of the key energy conversion components, high-power dc–dc converters play an important role in dc distribution systems and energy storage systems [6–9]. The dual active bridge (DAB) is a widely known topology for high-power dc–dc conversions with bidirectional power-transfer capability, high power density and zero voltage switching (ZVS) capability [10–13]. Dead time between the complementary driving signals is needed to avoid short circuit in DAB converter, however, dead-time effect of the modulation process leads to output voltage distortion and circulating current generation, which has become an apparent issue in high-switching-frequency high-power DAB DC-DC converter [14–17].

Recently, many researches have tried to resolve the above problem. In [18], segment-dividing model of Phase-shifted full-bridge converter is proposed and dead time expression is optimized, which broadens soft-switching range. In [19], dead time optimization expression is proposed, however, it does not consider minimizing the leakage inductor current RMS. In [20], the optimal dead time is determined by a large number of experiments in a specific converter, but theoretical analysis is not provided for specific optimization methods. In [21], a simple dead time compensation method is proposed, which requires additional hardware circuits to detect conducting time of the converter transistor, as a result, the hardware circuit complexity of the converter is increased. In order to save hardware costs, a dead time compensation strategy based on voltage space vectors is proposed, but it is incompatible with other modulation methods [22]. Additionally, in [23], a dead time compensation strategy based on volt-time equivalent principle is proposed, and the complexity of the control system can be decreased. In [24], the loss in dead time is analysed in detail, the switching losses can

be reduced, and the system efficiency can be improved. In [25], a multi-objective optimization method of leakage inductor current and ZVS range is presented. In [26], peak current is selected as the target under TPS control to achieve low conduction loss, which simplifies calculation and optimizes process. Unfortunately, all the above-mentioned modulation schemes fail to consider the existence of dead time, which seriously affects the safe operation of DAB.

According to the current direction of the bridge, a dead time compensation strategy for the modulation signal is proposed, which is based on the influence of dead-time effect on the output voltage of DAB converter. Furthermore, an Optimized Triple Phase-shift strategy is adopted, to make DAB converter operate under the minimum current stress, and the control curve of minimizing leakage inductor current RMS control is derived in detail, which is based on leakage inductor current RMS and zero voltage switching (ZVS). According to the curve, transformer secondary side duty-cycle is controlled to realize minimizing leakage inductor current RMS and soft-switching, which avoids phase-shift errors caused by Dead-Time Effect. the minimum current stress and soft-switching operation can be guaranteed, and the transfer efficiency of DAB converter can be improved. Finally, the simulation model as shown in Figure 1 is established in the MATLAB/Simulink, the experiment platform is built, and the proposed dead time compensation strategy is verified by simulation and experiment.

2 Dead Time Mechanism and Dead Time Effect

2.1 Dead Time Mechanism

The topology of bidirectional isolated DAB converter is depicted in Figure 1, which is constructed by two full bridges and a high-frequency isolated

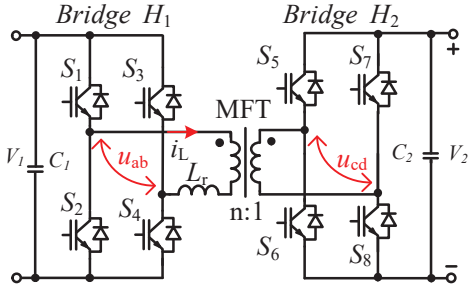


Figure 1 Topology of bidirectional isolated DAB converter.

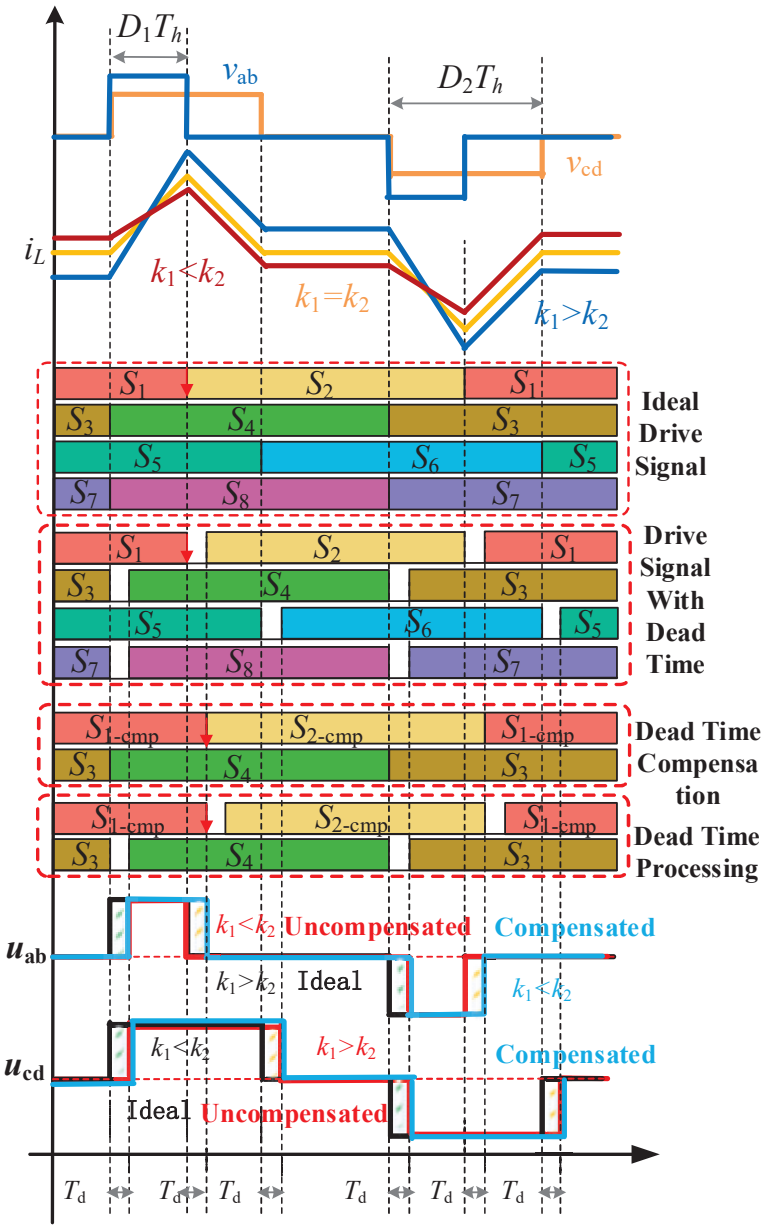
transformer with the turns ratio n:1. V_1 and V_2 denote separately input voltage and output voltage of DAB converter, MFT denotes intermediate frequency isolation transformer, u_{ab} and u_{cd} are ac output voltages of two bridges H_1 and H_2, respectively denote leakage inductance of the transformer, i_{L} denote the current of L_r, and T_{s} denote the switching cycle. On/off states of the switching devices S_1 and S_2, S_3 and S_4, S_5 and S_6, S_7 and S_8 are complementary. In order to avoid that V_1 and V_2 are directly applied to a single switch device, which will cause a short-circuit between the complementary driving signals, to avoid shoot-through phenomenon and guarantee the reliability of the converter, dead time is necessary to be inserted between the interlocked switches in the same bridge. There are two sequences in the three-level drive circuit of H-bridge structure, taking the primary side three-level as an example, there are $S_1S_3 \rightarrow S_1S_4 \rightarrow S_2S_4 \rightarrow S_2S_3 \rightarrow S_1S_3$ (defined as "mode 1") and $S_2S_4 \rightarrow S_1S_4 \rightarrow S_1S_3 \rightarrow S_2S_3 \rightarrow S_2S_4$ (defined as "mode 2"). Take mode 1 as an example, when S_3 turns off, S_4 will not turn on immediately due to the existence of dead-time effect.

2.2 Dead Time Effect

To simplify the following derivation, some assumptions are made as follows: Dead time is defined as T_{d}, when power is transmitted from *ab* side to *cd* side, it is defined as forward power transfer. Transformation ratio of controller is k_1, conversion ratio between the actual input and output voltage is k_2, primary side duty ratio is defined as D_1, and secondary side duty ratio is defined as D_2. Taking primary H-bridge structure (mode 1) as an example, the influence of dead-time effect on the bridge voltage is analysed.

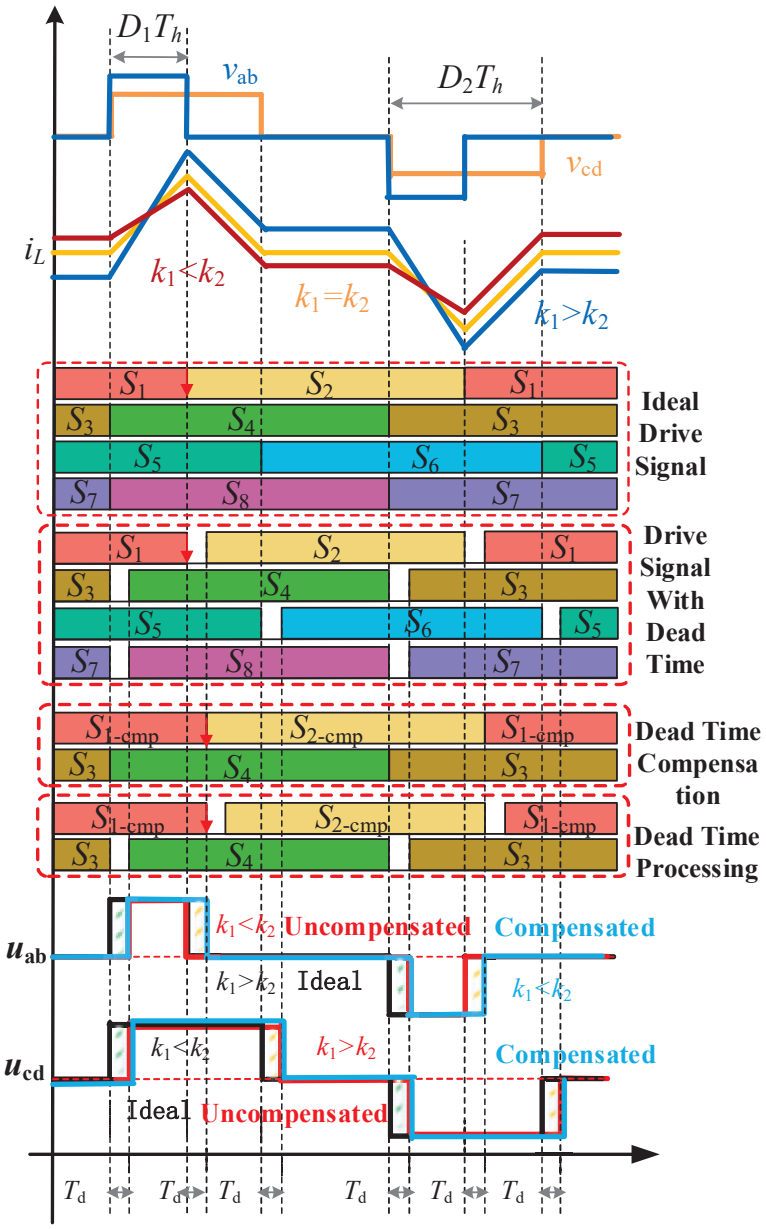
Under the conditions of $k_1 < 1$ and $k_2 < 1$, $D_1 < D_2$, the waveform of the transformer current i_L is shown in Figure 2.

During forward power transfer, the rising edge of the positive half-cycle of u_{ab} is taken as the initiation point of a current cycle (align edge of u_{ab} and u_{cd}). When the initial current is negative, dead-time effect has no effect on u_{ab}, and the phase of u_{cd} is delayed for one T_{d} because of dead-time effect, as shown in Figure 2(a) "$k_1 > k_2$ uncompensated u_{cd}". When the initial current is positive, dead-time effect has no effect on u_{cd}, and the pulse width of u_{ab} is decreased by one T_{d}, as shown in Figure 2(a) "$k_1 < k_2$ uncompensated u_{ab}". As a result, the transformer current is advanced to cross zero, circulating current is found on the secondary side of transformer, and DC offset is generated by transformer current.



(a) Forward power transfer

Figure 2 Continued



(a) Forward power transfer

Figure 2 The influence and compensation of dead-time effect.

Table 1 The influence of dead-time effect on bridge voltage

Power Transfer Direction	Initial Current Direction	The Influence of Dead-time Effect	
		u_{ab}	u_{cd}
Forward	Positive ($k_1 < k_2$)	Pulse width decrease: one T_{d}	No influence
	Negative ($k_1 > k_2$)	No influence	Phase lag: one T_{d}
Reverse	Positive ($k_1 < k_2$)	No influence	Phase lag: one T_{d}
	Negative ($k_1 > k_2$)	Pulse width Increase: one T_{d}	No influence

During reverse power transfer, the falling edge of the positive half-cycle of u_{ab} is taken as the initiation point of a current cycle(align edge of u_{ab} and u_{cd}). When the initial current is negative, dead-time effect has no effect on u_{cd}, and the pulse width of u_{ab} is increased one T_{d} because of dead-time effect, as shown in Figure 2(b) "$k_1 > k_2$ uncompensated u_{ab}", as a result, the transformer current is delayed to cross zero. When the initial current is positive, dead-time effect has no effect on u_{ab}, and the phase of the u_{cd} is delayed for one T_{d}, as shown in Figure 2(b) "$k_1 < k_2$ uncompensated u_{cd}".

Based on the above analysis, output voltage distortion and circulating current generation are caused by dead-time effect in the modulation process. Therefore, it is necessary to compensate for dead-time effect. The specific impact of dead-time effect on the bridge voltage is as summarized in Table 1, the influence of dead-time effect on the bridge voltage of the primary side is the pulse width, and the influence on the bridge voltage level of the secondary side is the phase.

2.3 Dead Time Compensation Strategy

From the above analysis, it can be found that there are three types of influence of dead-time effect on the bridge voltage: phase lagging, pulse width increasing and pulse width decreasing.

During forward power transfer, when the initial current is positive ($k_1 < k_2$), the pulse width of u_{ab} is decreased by T_{d}, as shown in Figure 2(a). Therefore, it is necessary to increase one T_{d} pulse width that is, the falling edge of the driving signal of the switching device S_1 is delayed for one T_{d}, as shown in Figure 2(a)" Dead Time Compensation S_{1_cmp} and S_{2_cmp}"

During reverse power transfer, When the initial current is negative ($k_1 > k_2$), the pulse width of u_{ab} is increased by one T_{d}, as shown in Figure 2(a). Therefore, it is necessary to increase one T_{d} pulse width, that is,

the falling edge of the driving signal of the switching device S_3 is delayed one T_{d}, as shown in Figure 2(b) "Dead Time Compensation S_{3_cmp} and S_{4_cmp}".

Comparing compensated bridge voltage level with ideal bridge voltage level, the pulse width of each voltage level is the same, however, compensated bridge voltage level lags behind ideal bridge voltage level by one T_{d} in phase, and the phase lag can be compensated by phase delay.

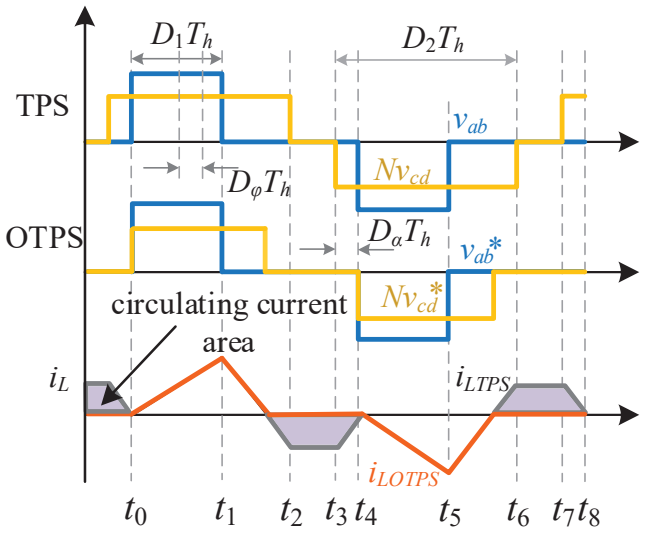
3 Modulation Methods

In order to improve the system efficiency by reducing switching loss and conduction loss simultaneously, an Optimized TPS modulation method is proposed. Figure 3 depicts the typical operating waveforms of DAB converter under TPS control and OTPS control, respectively.

3.1 TPS Modulation

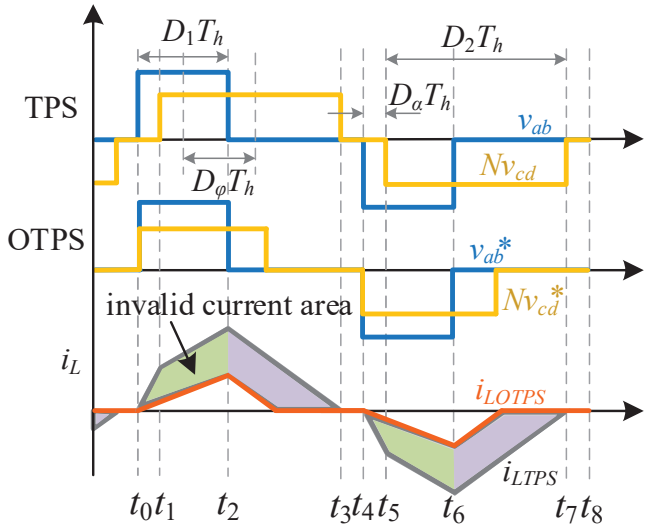
The phase-shift angle between the positive level midpoint of u_{ab} and u_{cd} is defined as $D_\alpha \pi$.

$$D_\alpha = \frac{1}{2}(D_1 + 2D_\varphi - D_2) \tag{1}$$

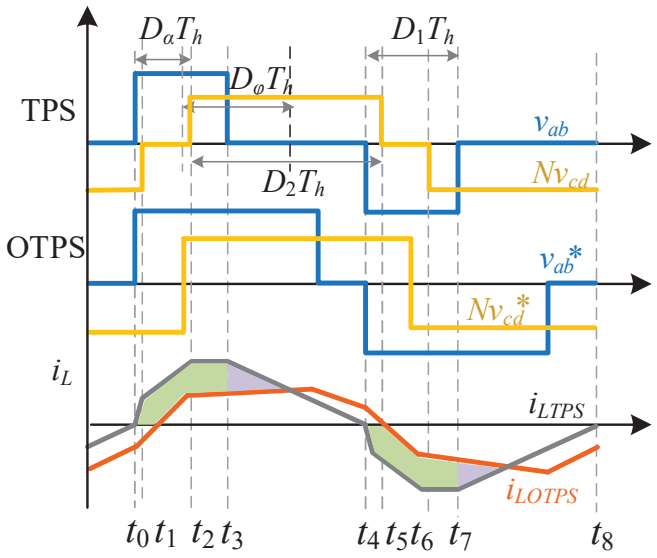


(a) Mode A

Figure 3 Continued



(b) Mode B



(c) Mode C

Figure 3 Operating waveforms of DAB under the TPS and OTPS.

Based on the rising edge of u_{ab} from 0 to U_1/2, as the rising edge of u_{cd} from 0 to U_2/2 moves backward, D_α is Slowly increases. There are three main operating modes of the circuit: mode A, mode B and mode C.

3.2 OTPS Modulation

As shown in Figure 3, DAB under TPS modulation strategy has problems such as large leakage inductance current stress and circulating current. In order to further reduce the current stress, improve the dynamic response performance, and eliminate circulating current and realize ZVS soft-switching of all switches over a wide operation range, it is necessary to optimize TPS modulation strategy. The optimized modulation parameters D_1, D_2 and D_φ are selected to further reduce leakage inductor current RMS under the condition ZVS. In addition, leakage inductor current RMS is reduced to zero at no-load.

(1) Mode A

The expression of leakage inductor current RMS in mode A is $i_L^* = f_A(k, P^*, D_1, D_2)$. In the formula, D_1 and D_2 are respectively solved to make the two partial derivatives zero, and D_1 and D_2 that minimize leakage inductor current RMS are obtained.

$$\begin{cases} D_1 = \dfrac{2k}{1-k} D_\varphi \\ D_2 = \dfrac{2}{1-k} D_\varphi \end{cases} \quad 0 < D_\varphi \le \frac{1-k}{2} \tag{2}$$

The operating waveform of OPTS in mode A is as shown in Figure 3(a).

(2) Mode B

The expression of leakage inductor current RMS in mode B is $i_L^* = f_B(k, D_\alpha, D_2)$, D_2 is solved to make the partial derivative zero and D_α is arrived.

$$D_\alpha = 0 \tag{3}$$

The operating waveform of OPTS in mode B is as shown in Figure 3(b).

(3) Mode C

The expression of leakage inductor current RMS in mode C is $i_L^* = f_C(k, P^*, D_1, D_2)$. In the formula, D_1 and D_2 are respectively solved to make

the two partial derivatives zero, and D_1 and D_2 that minimize leakage inductor current RMS are obtained.

$$\begin{cases} \begin{cases} D_1 = \dfrac{2D_\varphi + k - 1 + \sqrt{M}}{k} \\ D_2 = 1 \end{cases} & D_{\varphi 1} < D_\varphi < D_{\varphi 2} \\ \begin{cases} D_1 = 1 \\ D_2 = 1 \end{cases} & D_{\varphi 2} < D_\varphi < 0.5 \end{cases} \tag{4}$$

Where, $M = 4(k^2+1)D_\varphi^2 - 4(k^2-k+1)D_\varphi + 2k^2 - 2k + 1$, phase-shift duty-cycle dividing points $D_{\varphi 1}$ and $D_{\varphi 2}$ are expressed as:

$$\begin{cases} D_{\varphi 1} = (1-k)/2 \\ D_{\varphi 2} = 1/2 - (1 - \sqrt{1-k^2})/2k \end{cases} \tag{5}$$

The operating waveform of OPTS in mode C is as shown in Figure 3(c).

Figure 4 shows control block diagram of DC-DC converter. A difference value ($V_2^* - V_2$) is obtained by comparing the actual value V_2 with the reference value V_2^*, and phase-shift ratio D_φ is regulated by PI controller, then D_1 and D_2 are obtained by Equations (2), (4), (5) and (6), respectively, D_φ, D_1 and D_2 are input to the modulation module, and drive signals S_1–S_8 are obtained through modulation operation, dead time of the driving signals S_1–S_8 is used to process in dead time compensation module. According to the direction of the bridge current, the rising edge or falling edge of the driving signal is selected to reasonably compensate dead time, the compensation

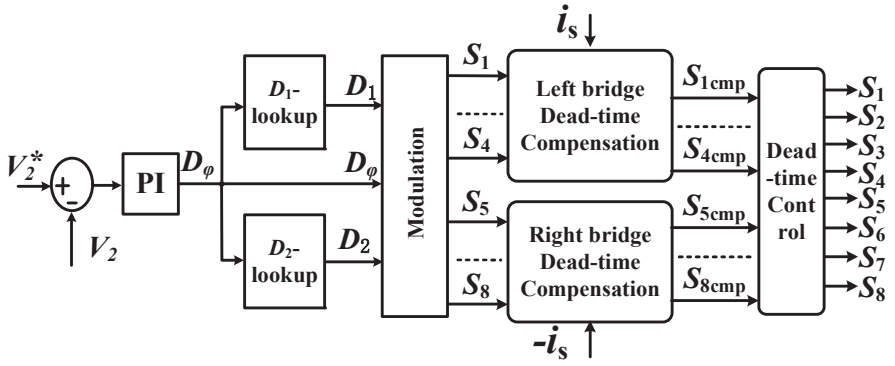


Figure 4 Control block diagram of DC-DC converter.

signal is output to dead time processing module to obtain the driving signals S_1–S_8 of the switches.

4 Experimental Verification

4.1 Simulation Verification

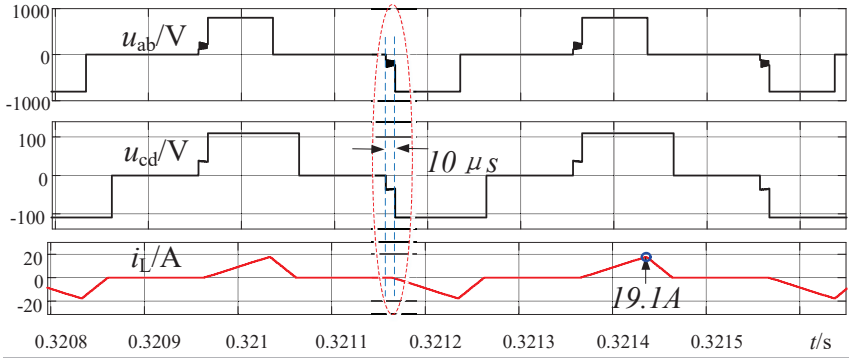
The simulation model of bidirectional isolated three-level DC-DC converter shown in Figure 1 is established in MATLAB/Simulink, and the simulation parameters are listed in Table 2.

Figure 5 illustrates the simulation results of dead time compensation.

Figure 5(a) gives the simulation results of voltage u_{ab}, voltage u_{cd} and current i_{L}, when dead time is not compensated in forward power transfer.

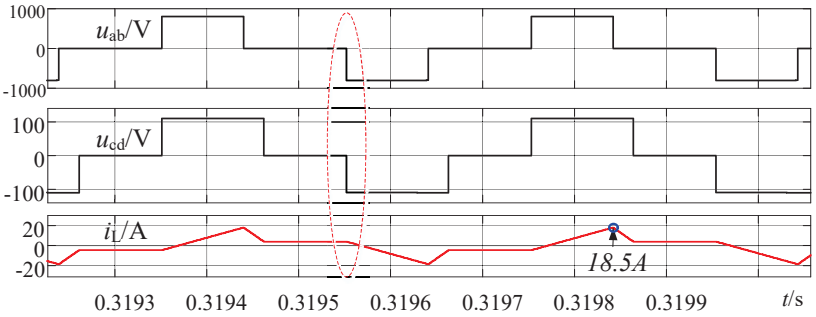
Table 2 The parameter of dead time compensation simulation

Simulation Parameters	Value
Rated Power	250 kW
Input DC Voltage	800 V
Inverter Output Voltage RMS	120 V
DC Capacitor C_1/C_2	4000 μF
Switching Frequency	10 kHz
Dead Time	2 μs
Leakage inductance	4 μH
Leakage inductor resistance	8.8 mΩ

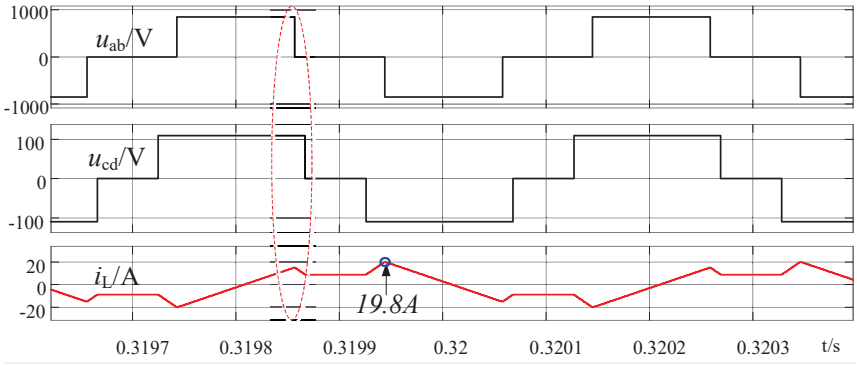


(a) Uncompensated dead time in forward power transfer

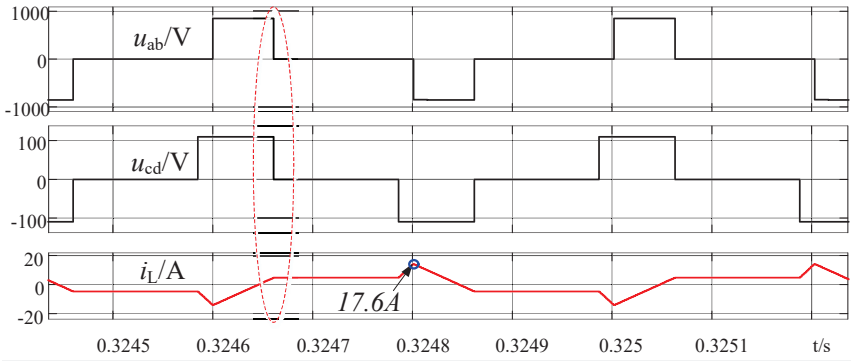
Figure 5 Continued



(b) Compensated dead time in forward power transfer



(c) Uncompensated dead time in reverse power transfer



(d) Compensated dead time in reverse power transfer

Figure 5 The simulation results of dead time compensation.

Figure 5(b) gives the simulation results of voltage u_{ab}, voltage u_{cd} and current i_{L}, when dead time is compensated in forward power transfer.

Figure 5(c) gives the simulation results of voltage u_{ab}, voltage u_{cd} and current i_{L}, when dead time is not compensated in reverse power transfer.

Figure 5(d) gives the simulation results of voltage u_{ab}, voltage u_{cd} and current i_{L}, when dead time is compensated in reverse power transfer.

By comparing the waveforms of voltage u_{ab}, voltage u_{cd} and current i_{L} in the case of dead time compensation in forward power transfer and reverse power transfer, the conclusions are as followed. When dead time is not compensated, the waveforms of voltage u_{ab} and voltage u_{cd} are not square waves, voltage sag and duty-cycle abnormality occur in dead time, phase relationship between voltage and current is changed, and the zero-crossing point of transformer current is not at the time when the polarity of H-bridge output level changes, duty-cycle is lost by 10μs in forward power transfer. After dead time is compensated, there is no loss of duty-cycle. In forward power transfer, leakage inductance current is decreased from 19.1A to 18.5A, a decrease of 3.14 per cent. In reverse power transfer, leakage inductance current is decreased from 19.8A to 17.6A, a decrease of 3.14 per cent. The waveforms of voltage u_{ab} and voltage u_{cd} are square waves. There is no voltage offset in dead time. Zero-crossing point of the transformer current happens at the time when the polarity of H-bridge output level changes, therefore, period decoupling of adjacent switching is ensured, and good soft-switching performance can be achieved, so that the accurate control of the average current transmitted at the AC side can be realized, and current distortion at the grid side can be suppressed; at the same time, circulating current is eliminated, which contributes to the improvement of system efficiency. The simulation results verify that the proposed control strategy is correct and effective.

In order to verify the effect of OTPS modulation strategy on improving system efficiency, The curves of leakage inductor current RMS with respect to transmission power under OTPS, TPS and phase-shift control are compared in Figure 6. The transmission power of the converter changes from no-load to full load. Leakage inductor current RMS in no-load condition is about 48A and 80A under TPS and phase-shift control, under OTPS control, leakage inductor current RMS in no-load condition is close to 0, and leakage inductor current RMS under light-load operation is the smallest. The simulation results are consistent with theoretical analysis, which shows that OTPS modulation strategy effectively improves the system efficiency by eliminating circulating current and optimizing transformer current RMS.

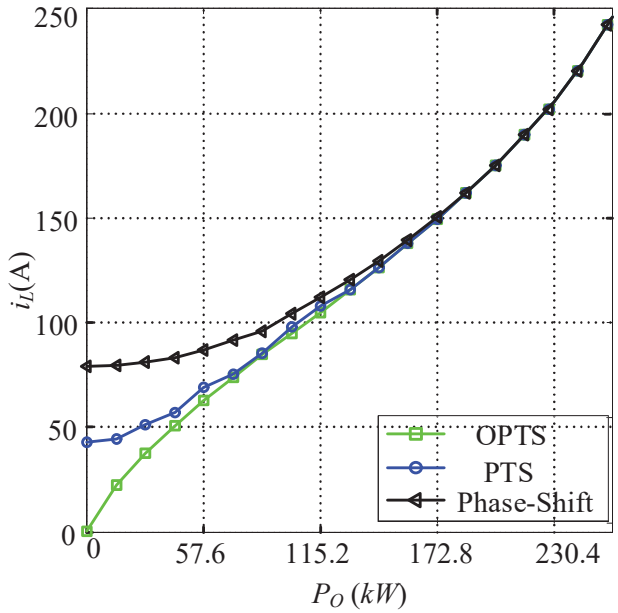


Figure 6 Comparison curve of leakage inductor current RMS under OTPS, TPS and phase-shift control.

4.2 Experimentational Verification

In order to further verify the correctness and effectiveness of the proposed dead time compensation strategy, Prototype photograph of the DAB system shown in Figure 7 is built according to DC-DC converter shown in Figure 1. FPGA chip EP3C55F484I7 was selected as the main controller, Verilog is used to design the proposed dead time compensation strategy. The parameters of the experimental system are listed in Table 3.

The static experimental results of dead time compensation are shown in Figure 8. Figures 8(a) and 8(b) demonstrate the experimental results of voltage U_0, voltage u_{ab}, voltage u_{cd} and current i_{L} under uncompensated dead time and compensated dead time in forward power transfer respectively. Figures 8(c) and 8(d) demonstrate the experimental results of voltage U_0, voltage u_{ab}, voltage u_{cd} and current i_{L} under uncompensated dead time and compensated dead time in reverse power transfer respectively. The output voltage is distorted under uncompensated dead time, the output voltage is a complete square wave under compensated dead time, and ZVS soft-switching of all switches over a wide operation range are realized. In forward power

Table 3 Main Parameters of dead time compensation experiment

Experimental Parameters	Value
Input DC Voltage	120 V
Inverter Output Voltage RMS	20 V
Switching Frequency	10 kHz
Dead Time	2 μs
Auxiliary Inductance	1.5 mH
DC Capacitor C_1/C_2	100 μF
Input side MOSFETs	PT015N10N5
Output side MOSFETs	C3M0065090J

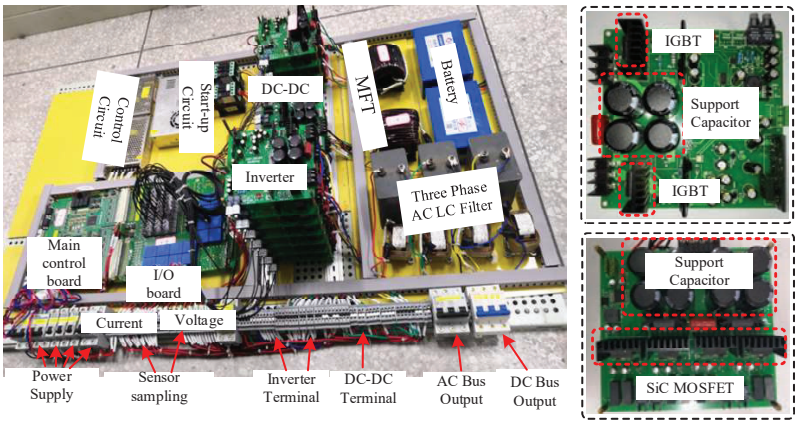
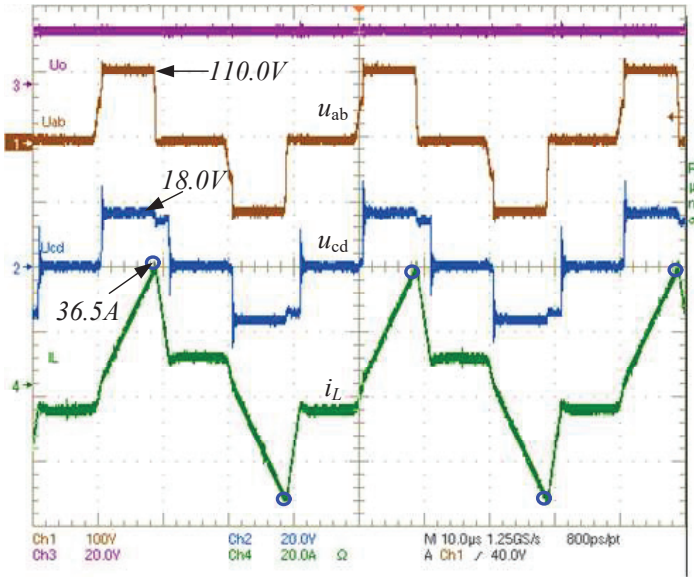


Figure 7 Prototype photograph of the DAB system.

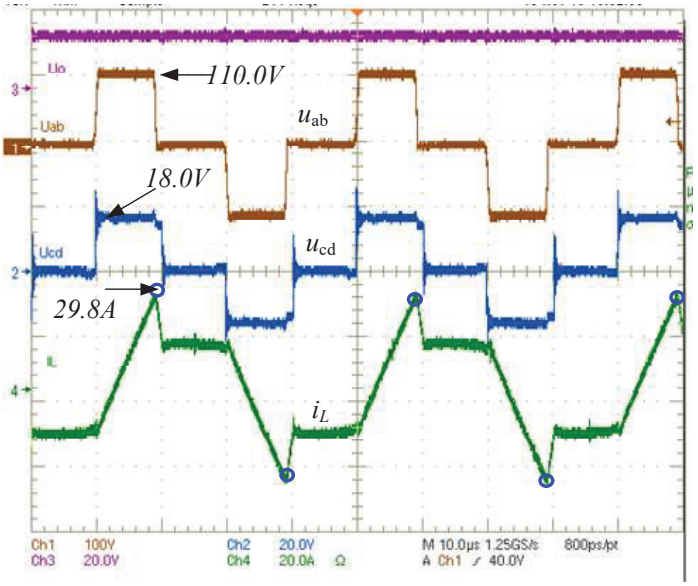
transfer, leakage inductance current is decreased from 36.5A to 29.8A, a decrease of 18.56 per cent. In reverse power transfer, leakage inductance current is decreased from 24.7 to 20.8A, a decrease of 15.79 per cent.

Figure 9 presents the results of the start-up experiment with $K_1 = 0.95$ and $U_{\rm dc} = 100$ V. Figure 9(a) shows that output voltage U_0 shakes during startup under uncompensated dead time, and the voltage fluctuates during operation. leakage inductance current increases by about 1.4A, and DC voltage stably outputs 20.4V for about 2.1s; Figure 9(b) shows that output voltage U_0 is always stable during startup under compensated dead time, and voltage and current do not fluctuate during operation. leakage inductance current increases by about 1.2A, and DC voltage stably outputs 20.4V for about 1.8s, which achieve a smoother dynamic waveform and a faster dynamic response.

Figure 10 illustrates stability of dead time compensation in forward circulating current. The compensation deviation threshold is 1%, and circulating

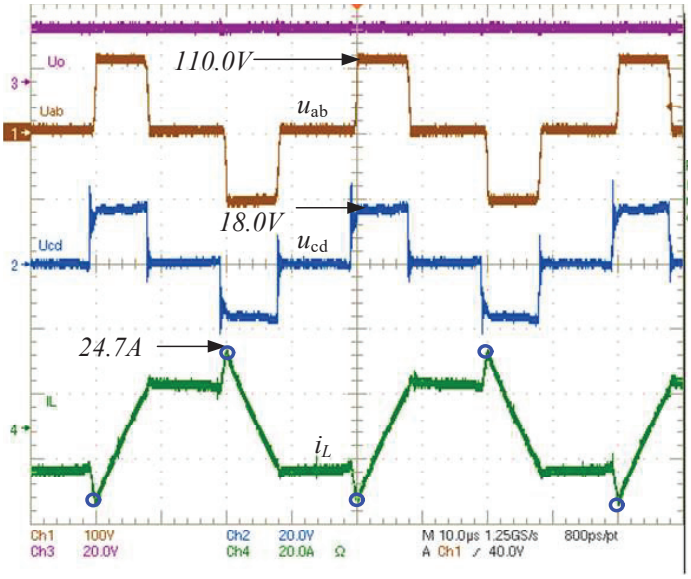


(a)Uncompensated dead time in forward power transfer

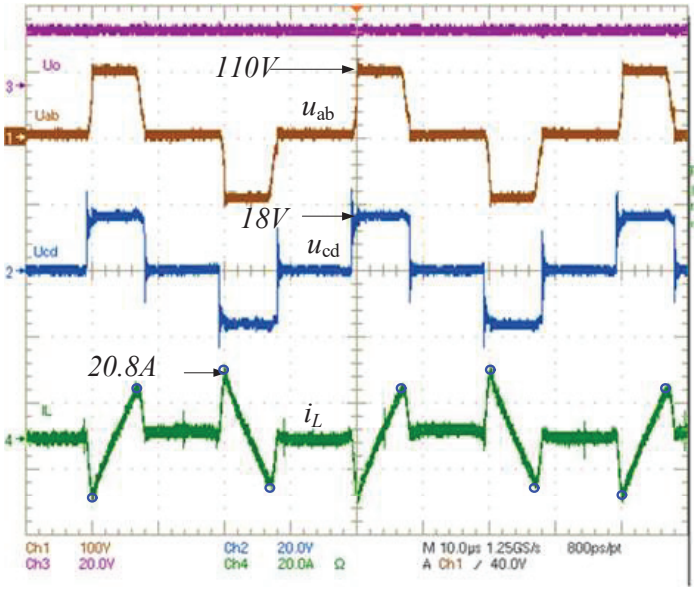


(b)Compensated dead time in forward power transfer

Figure 8 Continued

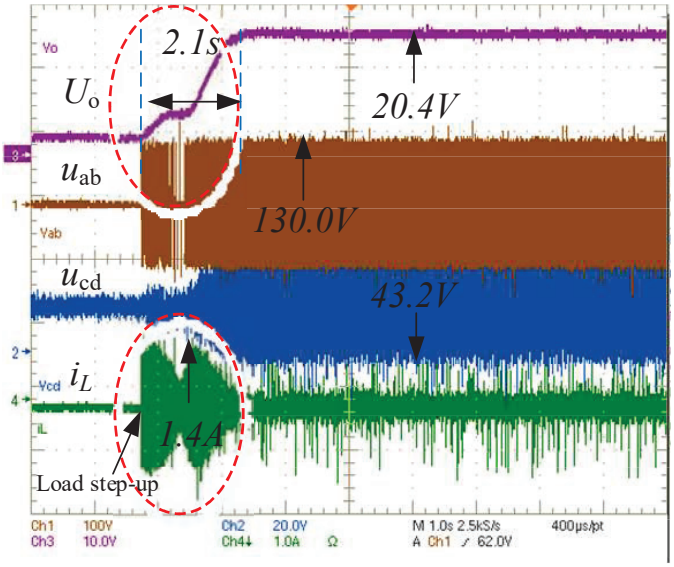


(c) Uncompensated dead time in reverse power transfer

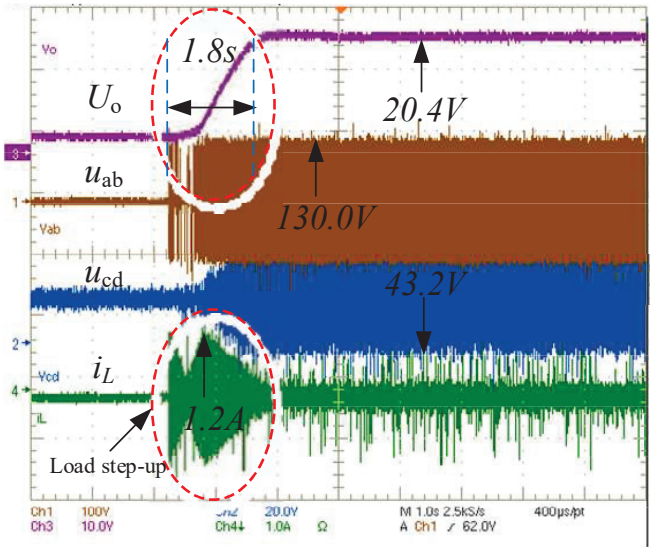


(d)Compensated dead time in reverse power transfer

Figure 8 The experimental results of dead time compensation.

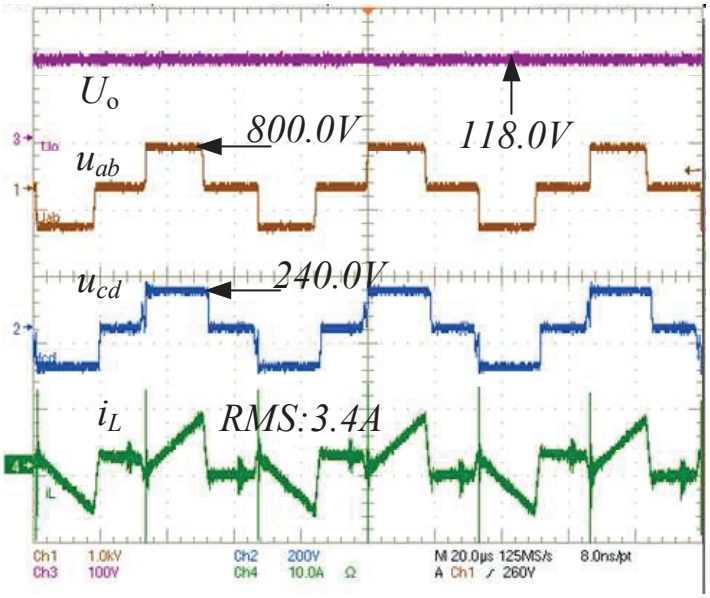


(a) Uncompensated dead time

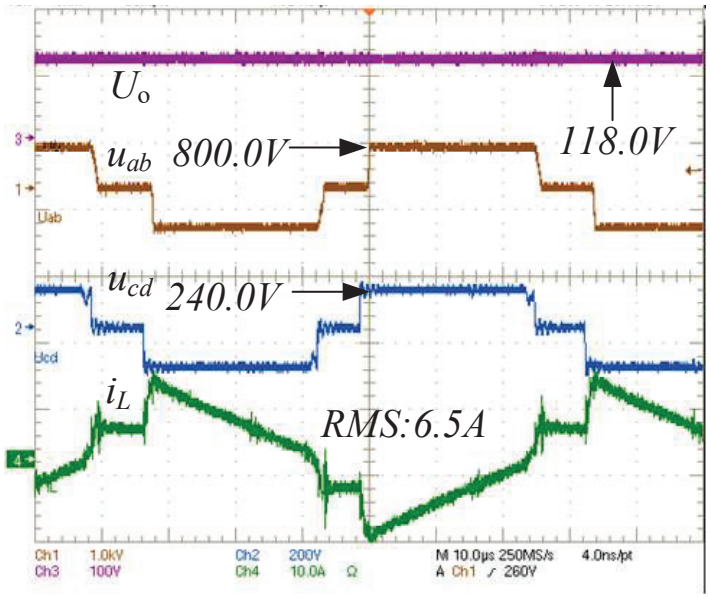


(b)Compensated dead time

Figure 9 Startup experiment.



(a) Forward circulating current (three level area)



(b) Reverse circulating current (phase-shift area)

Figure 10 Stability of dead time compensation in circulating current.

current is eliminated, which improves the system efficiency and ensures the decoupling of the transformer currents in adjacent switching periods, as a result, the accurate control of the AC side transmission current is realized, and current distortion is suppressed. The experimental results show that the proposed dead time compensation technology and OTPS modulation strategy are effective and feasible.

5 Conclusion

Aiming at the problem that dead time in the modulation process leads to output voltage distortion and circulating current generation, a dead time compensation strategy is proposed. An optimized TPS modulation strategy based on minimizing leakage inductor current RMS control is adopted. According to the expression of transformer leakage inductance current RMS and ZVS condition, control curve of minimizing leakage inductor current RMS control is derived. according to the control curve, the duty ratio of high-voltage side of the converter is controlled to minimize transformer leakage inductance current RMS, ensuring ZVS for switches and reducing the current stress over wide power and voltage ranges. The proposed dead time compensation strategies are verified by MATLAB simulations and experimental results on a downscaled DAB system.

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