Design and Implementation of Low-Cost PMU for Off-Nominal Frequency and DDC in Compliance with IEEE C37.118 Standard

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Abstract

The transition of the conventional power grid into the smart grid requires continuous monitoring of integrated grids speared over wide-area through Phasor Measurement Units (PMU). These PMUs additionally perform protection and state estimation functions in the smart grid. This paper discusses implementation of a new phasor estimation method to eliminate the effects of Decaying DC (DDC) component and off-nominal frequencies during the extraction of the phasors from a relaying signal. The practical implementation of the proposed method in a low-cost microcontroller (ESP32-WROOM-32 development board) in compliance with the requirements of IEEE C37.118.1a-2011 standard is also demonstrated. The analysis of various existing algorithms estimating the phasors is carried out. The microcontroller is programmed with the best among the analysed algorithm and its feasibility to function

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as a proper Phasor Measurement Unit is tested. The newly designed PMU is rigorously tested with different estimation methods compliant with IEEE C37.118a-2011 standard. The comparison of the proposed method with different phasor estimation algorithms is also discussed.

Keywords: IEEE Standard-C37.118, PMU, smart grid, wide area protection, off-nominal frequency, decaying DC component.

Abbreviations

LDC	Load Dispatch Centre
SCADA	Supervisory Control and Data Acquisition system
EMS	Energy Management System
WAMS	Wide-Area Measurement System
PMU	Phasor Measurement Unit
ROCOF	Rate Of Change Of Frequency
GPS	Global Positioning System
DFT	Discrete Fourier Transform
SVA	Sample Value Adjustment
FCDFT	Full Cycle Discrete Fourier Transform
TVE	Total Vector Error

1 Introduction

Transmission networks are usually considered as the backbone of a large power system, and need to be monitored continuously for maintaining the sustainability of the complete system. Continuous monitoring requires fetching of information from the field such as analog and digital data (status of a circuit breaker, power flow and frequency) measured with the help of Current Transformer (CT), Potential Transformer (PT) and the circuit breaker (CB) at substation level. The CT and PT data at all the substations are collected and monitored at a remote unit called the load dispatch centre (LDC). During abnormal conditions, the load dispatch centre will generate the necessary preventive actions to avoid any system failure that can hamper electric grid continuity. Traditionally, analog and digital information is measured at the substation level and transmitted to the load dispatch centre using the Supervisory Control and Data Acquisition system (SCADA) that sometimes can also be referred to as Energy Management System (EMS) [1]. The major limitation of SCADA or EMS is the inability to estimate the phase angle between a

pair of substations accurately. At the same instance, with the recent increase in renewable energy integration to power grid and installation of supporting power electronics devices, creates a more challenges in relay coordination, circuit breakers tripping and reliability degradation during disturbances in the power system [2].

In recent years, modern power systems have seen the innovation of Wide-Area Measurement System (WAMS) for monitoring, control, and protection of the power system [3]. WAMS uses intelligent electronic devices such as Phasor Measurement Unit (PMU) to collect accurate and fast synchronized measurements of bus voltages, line currents, frequency, and rate of change of frequency (ROCOF) in the smart power grid. PMU overcomes the limitations of SCADA or EMS by accurately calculating the synchro phasors from substations located at distant locations [4]. The application of PMUs in a few protection schemes [5, 6] also helps in vanquishing the protection challenges caused due to injection of renewable power sources into the power grid.

PMUs are used for better and safer monitoring of Electric Power Systems (EPS) [7]. In EPS measurements of voltages and currents being collected from distant locations. Such measurements are performed by the PMUs, synchronized by Global Positioning System (GPS) satellite distribution. The synchronized phasor measurements help in wide-area monitoring, controlling, and help the relays to detect the faults for taking preventive measures in the power system network. In the present scenario, PMU now became the backbone of the wide-area power system protection, monitor, control, and improves the reliability of the system [8–10]. Upon knowing the importance of PMUs in power grid, the Indian government has started initiative known as "URTDSM", which aims to install a large number of PMUs at the optimal positions in Indian grid network [11].

PMUs are classified into two classes, P class and M class [12]. The P class PMUs are called a protection class, mainly focusing on the speed of estimation rather than accuracy. Further, M class PMUs are called the Measurement class which mainly focuses on accuracy. The Phasor estimation algorithms in PMUs can be broadly divided into Discrete Fourier Transform (DFT) and non-DFT-based methods. In DFT based methods many variants of DFT, such as interpolated Discrete Fourier Transform (IpDFT) [13–15], the Clarke transformation DFT (CT-DFT) [16], and quasi-positive-sequence DFT (Qps-DFT) [17], have been reported in the literature to estimate the phasors which are compatible with IEEE Std. C37.118.1a-2011 [12, 18]. However, the discussed techniques try to compensate for phasor computations during off-nominal frequencies in the power system frequency, but do not give

efficient computation. In non-DFT based methods the phasors are estimated using wavelet transform (WT) [19], short-time Fourier Transform (SFT) techniques [20, 21], Dictionary approach, [22–24], Hilbert transform [25] and Kalman–Fourier filter [26, 27]. The Wavelet transform approach [19] uses approximation coefficients extracted using db4 mother wavelet to estimate the phasors, but the WT method does not account for the effect of DDC in the system and dynamic phasor estimation. For improvement in dynamic phasor estimation, short-time Fourier Transform methods (SFT) are introduced [20, 21], which improves dynamic phasor estimation by blending the SFT with Taylor series derivatives. However, the drawback is the cost of increased computation burden, and the effect of decaying DC offset disturbance is also relatively high. For improvement in phasor estimation when Decaying DC offset is present in the power system signal, techniques such as Full Cycle DFT (FCDFT) with two extra samples [28] and Modified FCDFT [29], were introduced. The implementation of phasor estimation with modified DFT techniques reduces the effect of DDC in PMUs [15]. However, due to the common nature of DFT, the accuracy is affected badly during change in power system frequency. Other non-DFT based methods include such as Dictionary based Phasor Estimator [22–24] which utilizes stored dictionary matrices and applies least square method for estimation of phasors. However, all these [22–24] suffer during off nominal frequency inputs. The [25, 30] proposed the phasors estimation technique which can work in off-nominal frequencies as well. In [30] the fundamental component is extracted using the Hilbert transform and convolution, In [25], the phasors are estimated based on approximation of the K^{th} Taylor polynomial by means of the Taylor Kalman–Fourier filter. However, the coefficient determination of the higher-order polynomial model is computationally heavy and also the Kalman filters are much more sensitive to narrowband disturbance like low order harmonics and inter-harmonics [26]. There are some techniques to improve the results of off-nominal conditions. [27, 31] introduces the method of frequency tracking where the sampling rate is changed depending on the frequency, but the resulting phasor measurements are not referenced to absolute time. Also, the resampling technique in [31] uses the N+4 buffer size of samples in SVA, which increases the memory and computational burden for phasor estimation. [32, 33] introduces techniques for a variable DFT window depending on the estimated frequency. But this [32, 33] has more computational burden. The proposed methodology adds a separate block to compute the frequency with proper filtering and adjusting the samples and calculates the phasors using a computationally less burden algorithm. Thus,

the proposed methodology in this paper tries to extract the phasors even under off-nominal situations with a less computational burden.

PMUs available today use expensive microcontrollers, digital signal processors, or FPGAs to cater fast and accurate calculations required for the PMU. This paper discusses developing a simple P-class PMU on a low-cost microcontroller taking DDC and off-nominal system frequencies and harmonics into consideration. This is achieved by a not-so-complex but accurate phasor estimation algorithm with proper minimal software implementation by using some software techniques like multicore programming etc. The phasor is estimated by a modified full-cycle DFT [29] which considerably removes the effect of DDC; prior to this, the system frequency is estimated via peak to peak detection and a modified sample value adjustment (SVA) is applied to the input signal to compensate for off-nominal frequency. The heterogeneous use of low pass and high pass filters for harmonics and DDC filtering for frequency estimation is also discussed. The performance of the proposed algorithm is evaluated by tests mentioned in IEEE Std. C37.118.1a-2011 [12, 18]. Furthermore, the feasibility and timing analysis of the algorithm is done on Espressif's ESP32-WROOM development board which houses a dual-core CPU running at 160 MHz and is a cheap microcontroller.

The proposed paper majorly includes the following: (i) development of frequency estimation block, modified sample value adjustments block, and modified Full cycle DFT (FCDFT) block in python, (ii) development of a less computationally burden algorithm for estimation of phasors, (iii) developing a simple P-class PMU on a low-cost microcontroller taking DDC, off-nominal system frequencies and harmonics into consideration. This is achieved by a simple and accurate phasor estimation algorithm with proper minimal software implementation by using some software techniques like multicore programming etc. The hardware considered for this ESP32-WROOM, (iv) The results of phasors are tested as per C37.118 standard. The novelty of the paper lies in frequency estimation block, SVM block and proposed algorithm methodology which requires less computational burden.

The paper is organized as follows: Section 2 discusses different implementations of PMU with a brief introduction and its drawbacks. A small gist of the proposed methodology is also provided. Section 3 discusses the proposed methodology in detail with the block diagram. Section 4 describes the tests done and the results of the proposed methodology. Section 5 describes the hardware implementation of the algorithm and discusses the feasibility of the microcontroller used along with some results followed by the conclusion Section 6.

2 Overview of Different Algorithms for Phasor Estimation From the Existing Literature

2.1 Dictionary Based Phasor Estimator [22]

The Dictionary-based phasor estimator uses dictionary-based sparse matrices which store details regarding all the possible phase angles (i.e) 0° to 360° beforehand as dictionaries like in Equation (1) which is then used to calculate the phase angle with the concept that the multiplication of two signals having the same phase angle yields the maximum sum.

$$S_{pr} = \begin{bmatrix} P_{11}^{r} & P_{12}^{r} & \dots & P_{1u}^{r} \\ P_{21}^{r} & P_{22}^{r} & \dots & P_{2u}^{r} \\ \vdots & & \ddots & \vdots \\ P_{i1}^{r} & P_{i2}^{r} & \dots & P_{iu}^{r} \end{bmatrix} \tag{1}$$

where,

$\mathrm{P}_{\mathrm{iu}}^{\mathrm{r}} = sin(\omega t_i + \vartheta_{\mu}^{r})$, 'r' varies from 1 to M, 'i' varies from 1 to N, and 'u' varies from 1 to M,
ϑ_{μ}^{r} is a vector consisting of M samples varying from α_{r} to $(\alpha_{\mathrm{r}} + \mu)$ with a step size of μ,
α_{r} is a vector consisting of M samples varying from μ° to 360° with a step size of μ.

Estimation of the phase angle is divided into two stages, namely coarse estimation stage (M signals stored in matrix have large difference in phase angle, 3.6° used in [22] and fine estimation stage (signals with finer difference in phase angle is used). The magnitude of the input signal is then calculated using the least square approximation. The main aim of the algorithm discussed in [22] is to estimate phasors with a low sampling rate, hence reducing the cost of the PMU. But the drawback is for a few cases of DDC and off-nominal frequency the algorithm in [22] may not adhere to TVE in limits.

2.2 FCDFT With Two Extra Samples [28]

The FCDFT with two extra samples estimator uses the basic phasor estimator, the FCDFT, to initially estimate the phasors using conventional FCDFT algorithm and then uses extra two samples to estimate the DDC error calculated as in Equations (2), (3), after which the DDC can be calculated by $\mathrm{Ae}^{-1/\mathrm{q}}$ which then is subtracted from the calculated phasor to obtain the

fundamental phasor.

$$e^{-1/q} = \frac{(X_{real(N+2)} - X_{real(N+1)})cos(2\pi/N)}{(X_{real(N+1)} - X_{real(N)})cos(4\pi/N)} \tag{2}$$

$$A = \frac{1}{2}\frac{N(X_{real(N+1)} - X_{real(N)})}{cos(2\pi/N)e^{-1/q}(e^{-N/q} - 1)} \tag{3}$$

2.3 Modified FCDFT [29]

This FCDFT phasor estimator like the previous algorithm calculates the DDC separately and then subtract it from the calculated phasor to get the actual phasor but without using any extra samples. The calculated phasor is divided into even numbered sampled DFT and odd numbered sampled DFT which is then used to calculate DDC as in Equations (4)–(6), then by subtracting $\mathrm{I}_{\mathrm{DFT}}^{\mathrm{dc}}$ from the calculated phasor the actual fundamental phasor is calculated.

$$K = I_{DFT}^{even} - I_{DFT}^{odd} \tag{4}$$

$$E = \frac{K_{img}}{K_{re}sin(2\pi/N) - K_{img}cos(2\pi/N)} \tag{5}$$

$$I_{DFT}^{dc} = K(1 + Ee^{-j\frac{2\pi}{N}})/(1 - Ee^{-j\frac{2\pi}{N}}) \tag{6}$$

2.4 Proposed Methodology

The algorithm discussed in [22, 28, 29] (FCDFT with two extra sample algorithm [28], Modified FCDFT [29], Dictionary Based Phasor Estimator [22], has been reimplemented for comparison analysis using the python platform and tested according to IEEE C37.118.1-2011 standard. It is observed that the above-mentioned algorithm has limitations with respect to DDC and/or off-nominal frequencies. The proposed methodology tries to resolve the issues posed by the previous methods. It introduces two additional blocks for frequency estimation and sample value adjustment to minimize the errors during off-nominal frequencies which is then applied on top of modified FCDFT as discussed in next section.

3 Implementation of the Proposed Methodology

Techniques discussed in the literature suffer from issues related to off-nominal frequencies, Decaying DC components, etc. The authors in this

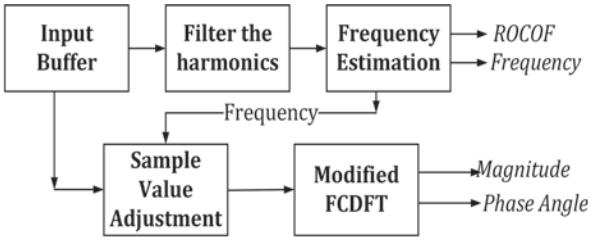


Figure 1 Block diagram of the proposed methodology.

paper try to resolve the above-defined problems. The proposed methodology deals with these problems by including a separate block for estimating the frequency and do necessary adjustments in the input signal such that it imitates a nominal frequency signal and then estimates the phasors using previously discussed DFT algorithms as opposed to other algorithms which calculated the frequency without any adjustment providing off frequency calculations.

The block diagram for the proposed methodology is shown in Figure 1 consisting of five main blocks as part of the proposed algorithm for estimating phasors. These include input buffer, harmonics filter, frequency estimator, SVA, and modified FCDFT. The input buffer stores or captures the sampled data points from the field, and these sampled data are then processed to estimate the frequency, which is given as one of the inputs to SVA to overcome the limitations caused due to the off-nominal frequencies in phasor estimation. Further, the output from SVA is given to the Modified FCDFT block to estimate the final phasors. The modified FCDFT block eliminates the problems caused to DDC during the phasor's estimation. The detailed description of blocks proposed in the algorithm is given in the following subsections.

3.1 Input Buffer

The input buffer is the sampled data (current or voltage) used, i.e., the output of ADC or stored dataset.

3.2 Filter the Harmonics

Filter is used to reduce the harmonics for accurate estimation of frequency (as harmonics alter the peak and zero-crossing timings of the signal). To do so a low pass Butterworth and a high pass Chebyshev filter having a cut-off

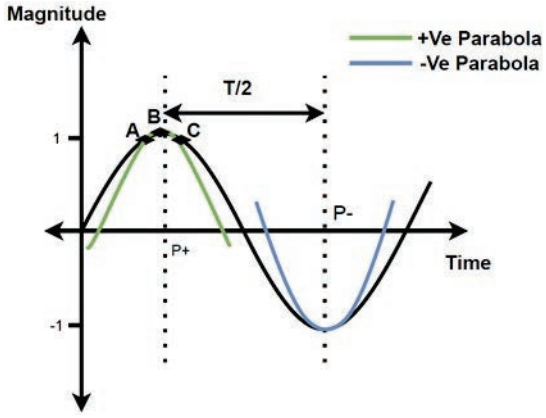


Figure 2 Peak timing estimation using parabola approximation.

frequency of 52 Hz and 48 Hz are used respectively to give us an effective bandpass filter. Different order combinations of filters have been tried and the best one has opted. The order of the filter is chosen to be 7 and 3 respectively.

3.3 Frequency Estimation

Frequency Estimation block uses the time between two peaks to estimate the frequency since full-cycle wave data is used. The location of peaks is critical to frequency and their detection is dependent on the sampled frequency to construct the discrete signal and hence may not be exact.

Therefore, a parabola approximation (interpolation technique) at extremes is used to estimate the underlying sinusoidal signal and to find the exact timings. If three points $A(x_1, y_1), B(x_2, y_2)$ and $C(x_3, y_3)$ are known, then the timing for the peaks can be found (as shown in Figure 2) using the equation:

$$2p = \frac{x_1^2(y_3 - y_2) + x_2^2(y_1 - y_3) + x_3^2(y_2 - y_1)}{x_1(y_3 - y_2) + x_2(y_1 - y_3) + x_3(y_2 - y_1)} \tag{7}$$

where p is the time corresponding to the peak with respect to the cycle. This parabola approximation is performed on both positive and negative half cycles present in a full cycle. This helps in identifying both positive and negative peak times in a cycle as per Equation (7). The frequency of the signal is estimated by using the change in two peak times. The estimated frequency can be used to find the rate of change of frequency (ROCOF).

3.4 Sample Value Adjustment

In most of the systems, the sampling rate is fixed which corresponds to the nominal frequency of 50 Hz/60 Hz. But when the system operates under off-nominal frequency conditions, DFT based algorithms suffer from the Spectral Leakage problem (when the sampling frequency does not produce the samples of full sample window). To overcome this and get the correct estimate of magnitude and phase angle, a Sample Value Adjustment Algorithm (SVA) is used which is an interpolation technique and transforms the input signal of any frequency to the nominal. For SVA, modification and "correction" in the derivation and the approach has been made to the algorithm presented in [29]. SVA shifts the sampled data of the off-nominal frequency signal to a nominal frequency signal which preserves the magnitude and phase angle. The spectral leakage problem is resolved as a result of shifting since the shifted signal is of nominal frequency and each shifted sampled data corresponds to the sampling rate of the nominal frequency.

The algorithm used for SVA is discussed below:

Assume an input signal X of frequency f_1

$$X = Acos(2\pi f_1 k\Delta T) \tag{8}$$

where,

k is sampled data index, i.e., 0,1,2,. . . ,N-1

N is the number of samples per cycle.

ΔT is the fixed sampling interval/ sampling time period, i.e, 1/(N$\times f_0$)

The shifted signal with the same amplitude and nominal frequency can be written as:

$$Y = Acos(2\pi f_0 k\Delta T) \tag{9}$$

Consider

$$\alpha = k\left(\frac{f_1 - f_0}{f_1}\right) \tag{10}$$

The basic equation for shifting can be written as:

$$Y(k) = X(k - \alpha) \tag{11}$$

Equation (11) shows that the value of kth samples for nominal frequency can be obtained by shifting the input signal by a factor of α.

To obtain an equation for shifting in terms of sampled data, we can use Taylor series expansion:

$$f(x) \simeq f(x_0) + f'(x_0)(x - x_0) + \frac{f''(x_0)(x - x_0)^2}{2!} \tag{12}$$

or

$$f(x-h) \simeq f(x) + hf'(x) + h^2 \frac{f''(x_0)}{2!} \tag{13}$$

We can write Equation (11) using Equation (13) as:

$$Y(k) = X(k-\alpha) \simeq X(k) + \alpha \Delta T X'(k) + (\alpha \Delta T)^2 \frac{X''(k)}{2!} \tag{14}$$

The derivatives can be computed using the central difference approach which is as follows:

$$\frac{dX(k)}{dt} = X'(k) = \frac{X(k+1) - x(k-1)}{2\Delta T} \tag{15}$$

$$\frac{d^2X(k)}{dt^2} = X'(k) = \frac{X(k+1) - 2X(k) + x(k-1)}{\Delta T^2} \tag{16}$$

Using Equations (15) and (16) in Equation (14):

$$Y(k) = \beta_1 X(k+1) + \beta_0 X(k) + \beta_{-1} X(k-1) \tag{17}$$

where,

$$\beta_1 = (\alpha - 1)\frac{\alpha}{2}, \quad \beta_0 = (1 - \alpha^2), \quad \beta_{-1} = (\alpha + 1)\frac{\alpha}{2}$$

Now, using Equation (17), $Y(k)$ can be calculated easily with sampled data and thus we can get the adjusted signal which can be used by the DFT algorithm to estimate the Magnitude and Phase angle correctly.

Figure 3 shows the effect of Sample Value Adjustment. The solid line is the off-nominal wave which is adjusted into an equivalent nominal frequency wave represented by the dotted line.

3.5 Modified FCDFT

The Input signal processed by SVA is fed to the phasor estimation step in order to calculate the phasor magnitude and angle as per the algorithm discussed in Section 2.3.

4 Compliance Tests and Their Results

The performance analysis of proposed methodology is done as per the test requirements provided in IEEE C37.118.1a-2011 standard [12,18]. The

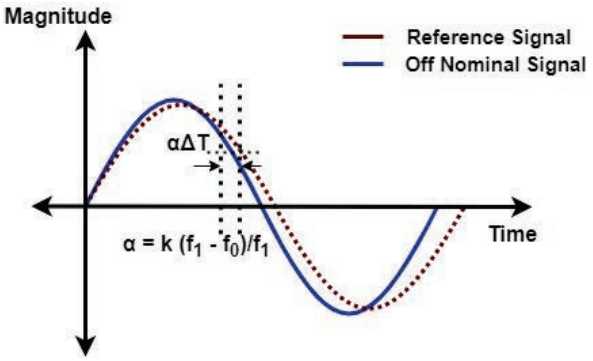


Figure 3 Sample value adjustment.

proposed methodology and the dataset for testing are developed using python. The dataset is created based on the pseudo flowchart mentioned in Figure 4. The presented work compares the proposed methodology with other estimators explained in Section 2, which were also implemented with python.

$$TVE = \sqrt{\frac{(\widehat{X_r}(n) - X_r(n))^2 + (\widehat{X_i}(n) - X_i(n))^2}{(\widehat{X_r}(n) + X_i(n))^2}} \tag{18}$$

As per the test requirements of the standard, the following compliance test signals, such as: (1) off-nominal frequency signal; (2) harmonics distorted signal; (3) phase and magnitude modulated signal; and (4) phase and magnitude step change signal are utilized to show the effectiveness of the proposed methodology. Along with the previously mentioned tests from the standard a decaying dc offset test (DDC) has also been performed. The accuracy of the estimators is shown and compared using the performance identifier known as Total Vector Error (TVE) (mentioned in standard) using Equation (18).

All test parameters considered in this paper are based on P-class PMUs. The signals used for testing are sampled at a sampling rate of 2.4 kHz (i.e) 48 samples/cycle for 50 Hz signal, which are fed to the proposed methodology along with other algorithms for estimation of phasor at a reporting rate of 50 frames/sec.

4.1 Decaying DC Offset Test

The presence of decaying dc components in fault current is one of the challenging issues in synchro phasor estimation algorithms. Typically, the amplitude of dc components varies from 30% to 90%, and its time constant

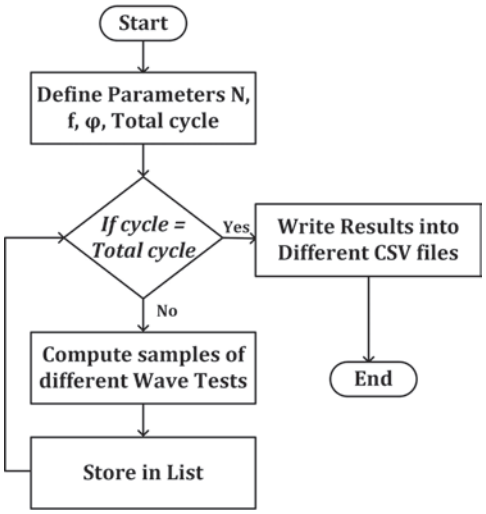


Figure 4 Flowchart followed for creating the dataset.

varies from 0.5 to 5 cycles depending on the fault resistance and network structure [29]. The mathematical expression, as given in the following equation, is used to simulate the effect of the presence of decaying dc component in a signal:

$$r_1(t) = R_m sin(2\pi ft + \theta) + \gamma e^{-t/\tau} \tag{19}$$

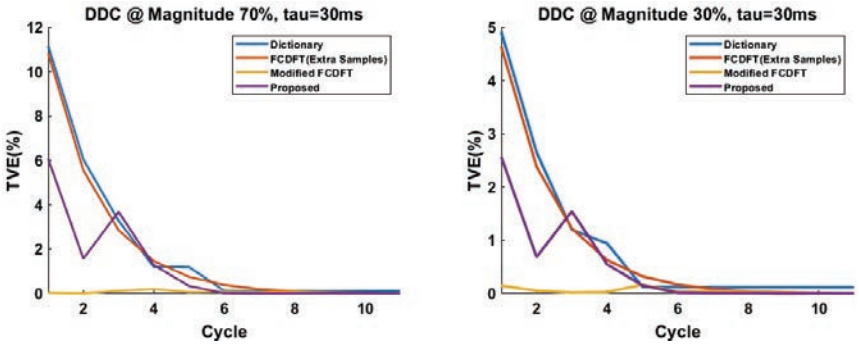
where γ and τ are the magnitude and time constant of the decaying dc component, respectively. The maximum TVE considered for this test is 3%.

4.1.1 Influence of magnitude of dc component

The magnitude (γ) is varied from 30% to 90% of $R_m = 150$ (input signal peak) at an interval of 20%, time constant (τ) = 30 msec, nominal frequency = 50 Hz and phase angle = 32°. Figure 5(a) gives a comparison of TVE for different algorithms discussed. As seen the modified FCDFT is almost immune to DDC, the proposed design is the 2nd best with slightly higher TVEs at the initial few cycles but other algorithms performed comparatively poorly.

4.1.2 Influence of time constant

Here, the time constant is varied from 10 to 100 msec at an interval of 30 msec with $\gamma = 135$ (90% of R_m), $R_m = 150$, $f_0 = 50$ Hz and $\theta = 32°$. Figure 5(b) gives the comparisons. This is also tested like the previous case but the results



(a) (b)

Figure 5 Shows the Comparison between different algorithms when DDC is present.

were similar like before with Modified DFT being the best and the proposed methodology being the second best.

4.2 Off-nominal Frequency Test

In practical situations, the grid has to maintain a constant 50 Hz frequency, albeit it's difficult to maintain and there will always be some deviations in the system frequency. This test shows the effectiveness of the proposed methodology when there is a deviation in system frequency. The equation used is:

$$r_2(t) = R_m cos(2\pi ft + \theta) \tag{20}$$

where f changes from 48 Hz to 52 Hz at an interval 0.25 Hz.

Figure 6 shows the comparison of different algorithms for off nominal frequency at 48 Hz (6.a), 49 Hz (6.b), 51 Hz (6.c), 52 Hz (6.d). As seen, the results of the proposed algorithm are way better than the others by keeping the TVE well within 1% required by the standard. Other in-between frequencies were also tested and similar results were seen.

For different frequency conditions, the maximum TVE and FE are shown in Figure 7. This shows for each case the maximum error which is 0.052% and 0.001Hz respectively.

4.3 Harmonic Distortion Test

This test shows the effectiveness of the proposed methodology when there are harmonics in the fundamental signal. The fundamental sinusoidal signal

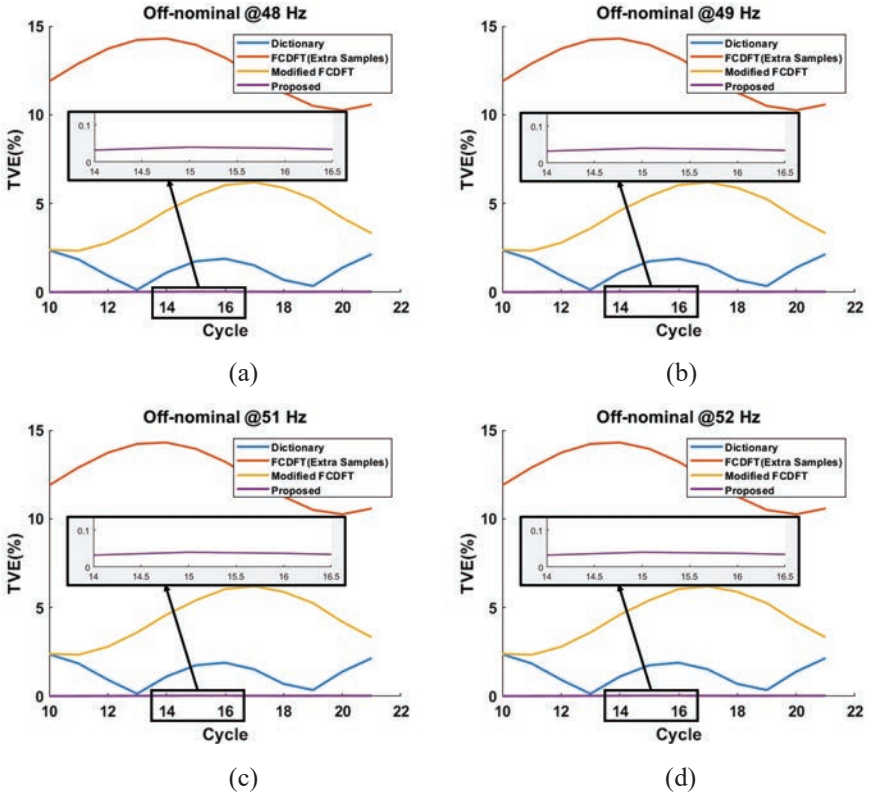


Figure 6 Comparison between different algorithms during different frequency conditions.

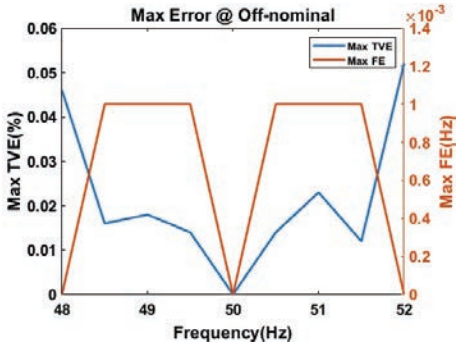


Figure 7 Maximum TVE and FE in off-nominal conditions.

with fundamental frequency 50 Hz along with the harmonics is represented in the following equation:

$$r_3(t) = R_m cos(2\pi f_o t + \theta) + \sum_{k=2}^{50} R_k cos(2\pi k f_o t + \theta_k) \tag{21}$$

where k is the harmonic order, R_k and θ_k are the peak amplitude and phase angle of the harmonic signal. The signal taken in order for the tests is a fundamental signal with 1% harmonics up to 50th order. The parameters used are: $R_m = 150$, $\theta = 32°$, $R_k = 0.01*150 = 1.5$, $\theta_k = 32°$. The maximum TVE in this case was observed to be 0.004%. All the other discussed techniques also performed well with very low TVE.

4.4 Modulation Test

This test shows the effectiveness of the proposed methodology when the system signal is amplitude and phase-modulated which can occur when there are unexpected power swings in the grid. The signal can be mathematically represented as:

$$r_4(t) = R_m(1 + K_x \sin(2\pi f_o t + \theta) \times \sin(2\pi f_o t + K_a \sin(2\pi f_m t) + \theta)) \tag{22}$$

where K_x and K_a are the modulated amplitude and phase coefficients respectively, and f_m is the modulation frequency. The common parameters used for both amplitude and phase modulation are: $R_m = 150$, $\theta = 32°$, $f_o = 50$ Hz and the modulating frequency is changed from 0 to 2 Hz with 0.25 Hz interval. For amplitude modulation the parameters considered are: $K_x = 0.1$, $K_a = 0$. For phase modulation the parameters considered are: $K_x = 0$, $K_a = 0.1$.

Figure 8 shows the TVE and FE of the proposed methodology for the test for different modulating frequencies. The TVE for amplitude modulation kept on increasing with an increase in f_m and crossed the 1% TVE border at higher frequencies but the FE is very less. In phase modulation, the TVE is well within the range, but with the increase in f_m the FE was increasing and crossed the border 0.06 Hz at higher frequencies. But both amplitude and phase modulation tests were within the range for most of the cases.

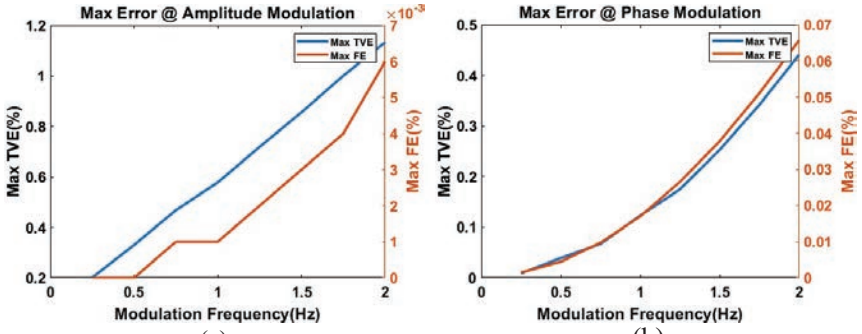


Figure 8 TVE and FE for modulation test of proposed methodology.

4.5 Step Test

This test shows the effectiveness of the proposed methodology when there is a sudden change in the input signal which can be caused when there are any faults in the system. The signal can be mathematically expressed as:

$$r_5(t) = R_m(1 + K_x U_1(t)) \sin(2\pi f_o t + \theta) \tag{23}$$

where K_x and K_a are the modulated magnitude and phase coefficients $U_1(t)$ is the unit step function. Both phase and magnitude step tests are done one at a time. The common parameters used are: $R_m = 150$, $\theta = 32°$, $f_o = 50$ Hz. For the magnitude step, $K_x = 0.1$ and $K_a = 0$ and the step input is applied between 1 to 1.1 sec at intervals of 20 msec. According to the parameters being used the maximum response time need to be less than 34 msec, the maximum delay time needs to be less than 5 msec and the overshoot should be less than 5%.

Figure 9(a) and (b) shows the result of the step change in amplitude applied at different cycles. The maximum response time, delay time and overshoot are 14 msec, 11 msec and 0% overshoot well within the requirements mentioned by the standard. Figure 9(c) and (d) shows the change in phase and TVE with respect to time when step change in phase is applied at different cycles. The maximum response time, delay time and overshoot are 21 msec, 15 msec and 0% overshoot. As seen the maximum delay time recorded is little off than the allowed limit from the standard because the filter is a little slow in the calculation of the phasors.

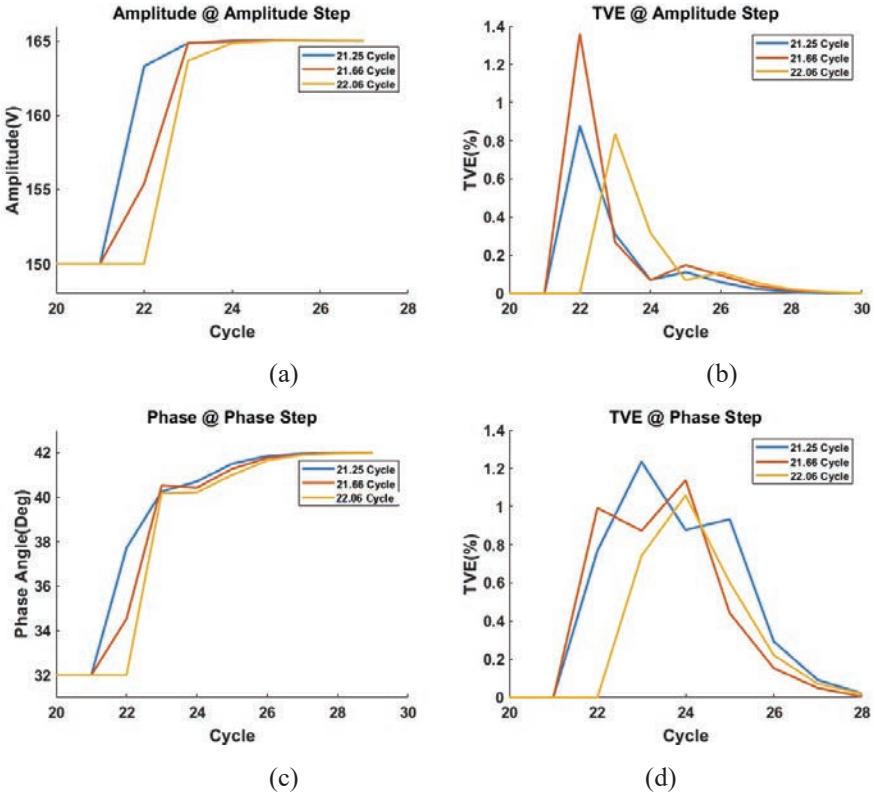


Figure 9 Step test performance for amplitude and phase.

5 Hardware Implementation

The proposed algorithm is also implemented on a microcontroller and tested for its feasibility. The microcontroller used is Espressif's ESP32-WROOM32 development board which has a dual-core microprocessor running at 160 MHz with a good number of peripherals and with many other features at a low price. The main advantages of ESP32 over other microcontrollers are its clock frequency, on-chip floating point unit, dual-core options, vector processor, and open-source support with matured libraries.

The proposed algorithm which is written in python is written again in Embedded C code as it has wide support for microcontrollers and is fast and efficient. The flashing of the proposed algorithm program on the microcontroller is done using Espressif's ESP-IDF extension in Visual Studio Code software present in the workstation. For testing the implementation,

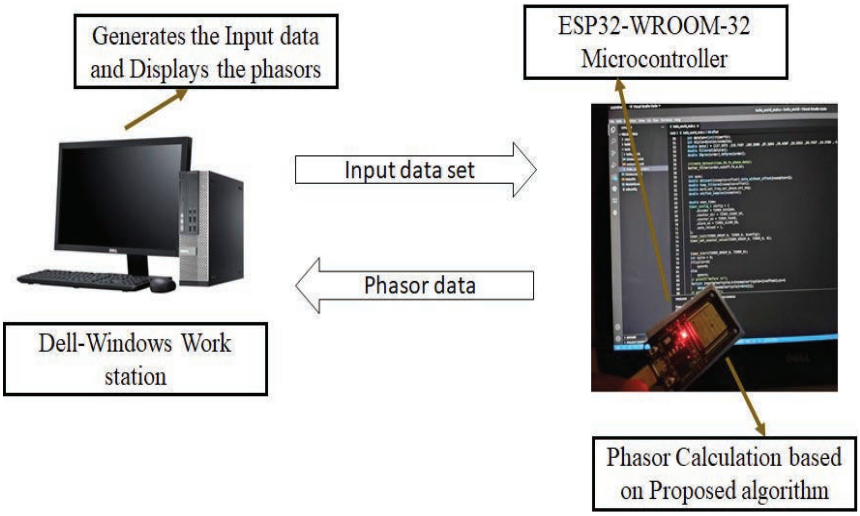


Figure 10 Block diagram of hardware implementation.

the dataset used in the simulations is transferred from the workstation and stored into the microcontroller memory which is taken by the algorithm and computes the phasor as shown in Figure 5.1. Further, the computed phasor data is transferred back to the workstation and displayed.

The target reporting rate is 50 frames/sec and to achieve this the microcontroller should be able to finish the computation of a cycle before the execution of the next cycle (i.e.) execution should not take more than 20 msec. So, a timer is set up to measure the computation time of microcontroller for one cycle. The execution time of one cycle is found to be 4.977 msec far below the required time, hence in spite of its low cost compared to microcontrollers used in commercial PMUs, the ESP32 is more than capable of handling the job with great accuracy.

All the test cases considered in the simulation are validated on ESP32-WROOM-32 microcontroller. To explain in detail two test cases are considered for discussion. The test cases are (i) when off-nominal frequency is applied (ii) DDC is applied to the data set. For the test-case-i, Table 1 shows the result with the dataset having off-nominal frequencies. The results shown in Table 1 are from cycle 5 because the initial 4 cycles are needed for stabilization of the filter. Only up to 8th cycle is shown as the data for more cycles to store on the microcontroller demands more memory.

The results of the proposed algorithm performed in the microcontroller for off-nominal frequency are well within the standard limits i.e the phasor

Table 1 Results from hardware when test inputs with off-nominal frequencies are applied

Cycle No.	f = 48 Hz Mag(V), Angle(°), Freq(Hz), ROCOF, TVE(%)	f = 49 Hz Mag(V), Angle(°), Freq(Hz), ROCOF, TVE(%)	f = 50 Hz Mag(V), Angle(°), Freq(Hz), ROCOF, TVE(%)	f = 51 Hz Mag(V), Angle(°), Freq(Hz), ROCOF, TVE(%)	f = 52 Hz Mag(V), Angle(°), Freq(Hz), ROCOF, TVE(%)
5	150.01, −40.051, 48.018, −1.506, 0.089	150.018, −3.961 48.988, 0.928 0.069	150.088, 32.131, 49.956, 3.508, 0.236	150.29, 68.23, 50.928, 6.155, 0.446	150.356, 104.322 51.905, 8.932, 0.611
6	150.03, −54.415 48.006, −0.589 0.033	150.007, −11.189 48.996, 0.378 0.02	150.026, 32.044 49.985, 1.436 0.079	150.098, 75.278 50.977, 2.439 0.151	150.056, 118.473 51.973, 3.405 0.133
7	150.028, −68.807 48.003, −0.131 0.022	150.003, −18.4 48.998, 0.13 0.002	150.0, 32.0 49.995, 0.511 0.0	150.033, 82.43 50.993, 0.812 0.057	149.995, 132.801 51.994, 1.045 0.004
8	150.026, −83.201 48.001, −0.118 0.017	150.001, −25.602 48.999, 0.038 0.004	150.0, 32.0 49.999, 0.165 0.0	150.011, 89.616 50.997, 0.233 0.029	149.972, 147.184 51.999, 0.255 0.034

estimated during different off-nominal conditionals has the TVE far less than the required standard percentage i.e 3%. Thus, the proposed methodology performs well for the different frequency changes and is able to give better results even in off-nominal frequencies.

For test case ii, Table 2 shows the result with the dataset having DDC. The results shown in Table 2 are from cycle 5 because the initial 4 cycles are needed for stabilization of the filter. Only upto 8th cycle is shown as the data for more cycles to store on the microcontroller demands more memory.

The DDC of different percentages are applied separately on the individual data set at the 5th cycle to show its effect on the TVE. As seen from the result when a DDC is applied to the dataset at a particular cycle algorithm takes 2 cycles of time to stabilize and to give better phasor results that are well within the standards i.e TVE is less than 3%.

Thus, the proposed algorithm works better for all different compliance tests present in IEEE c37.118.1 standard with exceptions in DDC for 2 cycles initial change and gives the results of phasor well within the limits as per standards requirements.

Table 2 Results from Hardware when test inputs with DDC

Cycle No.	30% Mag(V), Angle(°), Freq(Hz), ROCOF, TVE(%)	50% Mag(V), Angle(°), Freq(Hz), ROCOF, TVE(%)	70% Mag(V), Angle(°), Freq(Hz), ROCOF, TVE(%)	90% Mag(V) Angle(°), Freq(Hz), ROCOF, TVE(%)
5	152.462, 33.12, 49.625, −18.735, 2.565	154.128, 33.874, 49.374, −31.315, 4.309	155.791, 34.637, 49.122, −43.905, 6.075	157.427, 35.417,48.87, −56.48,7.863
6	148.96, 31.207, 50.176, 4.57, 1.544	148.239, 30.65, 50.297, 7.845, 2.62	147.538, 30.094, 50.42, 11.293, 3.685	148.206, 31.075, 50.248, 68.888, 2.001
7	149.39, 31.684, 50.085, 22.966, 0.684	148.993, 31.477, 50.14, 38.321, 1.131	148.6, 31.274, 50.195, 53.635, 1.569	146.832, 29.529, 50.546, 14.872, 4.761
8	149.573, 31.731, 50.063, −5.664, 0.548	149.281, 31.547, 50.105, −9.587, 0.923	149.015, 31.367, 50.148, −13.604, 1.282	148.743, 31.184, 50.192, −17.676, 1.647

6 Conclusion

The proposed methodology was compared with some of the techniques published in past and gave better results comparatively in most of the cases. The (synchro phasors) results of the proposed methodology follows the requirements mentioned in the IEEE standard C-37.118. The tests with DDC did not comply with the standard for the initial 2 cycles because the sudden change in input signal makes the estimated frequency to be little off which then introduces error after sample shifting. As the number of cycles increases the error starts to decrease and approaches within the limits as per standard. In step change also the maximum delay time was exceeding the limit. Both mentioned exceptions were mainly occurring because of the slow filter which needs to be improved for the next phase of work.

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