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# Design and Analysis of Quasi-Y Source High Gain DC/DC Resonant Converter for Renewable Energy Applications

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## Abstract

This paper proposes a magnetically coupled partial resonant isolated quasi-Y source DC/DC converter. Here, to achieve soft switching, there is no additional auxiliary circuits or magnetic components are used. By making use of transformer's parasitic elements like winding capacitance ( $C_p$ ) and leakage inductance ( $L_{kl}$ ), zero current switching (ZCS) is obtained at the turn-off instant of all MOSFETs. Hence, the converter can operate at a higher frequency, so that compact size and good efficiency are feasible. This converter inherits all the conventional impedance source converter features, and a higher gain is obtained by using three winding coupled inductor and isolation transformer with small shoot-through duty ( $d_{ST}$ ). Hence, the continuous input current (CIC) and galvanic isolation feature of this converter is most suitable for renewable energy applications. Also, the output voltage is regulated by changing the switching frequency. Finally, a 300 W prototype is designed and tested in the laboratory. The simulation, experimental results with mathematical and design analysis are provided.

**Keywords:** Renewable energy resources, impedance source converters, high voltage gain, DC/DC converters, zero current switching (ZCS).

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## 1 Introduction

Nowadays, demand for renewable energy resources is growing more popular due to extensive utilization of fossil fuels such as coal, gas, and oil. Hence, which leads to major environmental pollution, greenhouse gas emissions, and it has a significant global impact. However, there is a considerable mismatch between the availability of fossil fuels and energy demand. So to meet the energy demand and ecological concerns, renewable energy resources are best alternatives. These sources are mainly wind, Biomass, fuel cells, photovoltaic (PV) systems, etc. [1, 2]. Among these, Solar PV and Wind are good candidates because their universal availability, emission-free, and fuel cell are also most significant due to higher conversion efficiency. The output voltage of the aforementioned renewable energy resources is low, so to interface with DC grids, high step-up DC/DC converters are required [3]. High voltage gain can be achieved by using the traditional DC/DC boost converter. However, the converter needs to operate at higher duty (close to unity). So that, components will suffer from higher current and voltage stress. Conduction losses in the converter are more because of the longer conduction of the active switch. Furthermore, the diodes at the output side will conduct very short intervals, resulting in significant reverse recovery issues [4].

In the literature, different types of non-isolated and isolated topologies are available for high voltage boosting [5–7]. By using the coupled inductors, high gain can be achieved. In [8], a soft switched non-isolated three winding coupled inductor type DC/DC converter is presented for high step up renewable energy applications. Here, the three-winding coupled inductor creates more degree of freedom to attain high voltage gain. In renewable energy resources, isolated converters are used for high step-up voltage to overcome higher duty ratio and safety concerns. The isolated topologies like full-bridge, flyback, push-pull, etc., can obtain high voltage gain by changing the transformer's turns ratio [9–12]. However, the converters in [9, 11] are high gain voltage fed converters (VFC), whereas in [10, 12] are current fed converters (CFC). These converters have some limitations; in the VFC, there is a prohibition with short through of switches in the same leg, to avoid this small dead band is provided in between them. Whereas in CFC, the switches (top & lower) in the same leg triggered together (Shoot through). Otherwise, DC inductor gets opened and it causes high voltage stress on switches and the main circuit gets damaged. VFC are buck type, whereas CFC are boost converters and can't be used as buck-boost converters. To overcome this, impedance source converters (ISC) are introduced and here switches in the

same leg can be short-circuited or open circuited. Hence, the ISC can be operated as buck type, boost type, or both buck-boost types [13–15]. Furthermore, based on topological structure, the ISC can be classified as non-isolated [16–19] and isolated [21–27] type converters. To achieve higher gain a three-winding coupled inductor Y-source converter is proposed in [17], it has more freedom to attain high gain. However, due to the DIC nature of this converter not a good candidate for PV and fuel cell systems. Hence, to overcome this a CIC quasi-Y-source converter is presented in [18]. Furthermore, to reduce the voltage stress on the components and higher voltage gain a modified Y-source DC/DC converter is presented in [19]. Here, all the aforementioned converters are non-isolated, and not suitable for PV, fuel cell systems. Here galvanically isolated impedance source DC/DC converters are present due to safety concerns in PV systems and grid-tied converters.

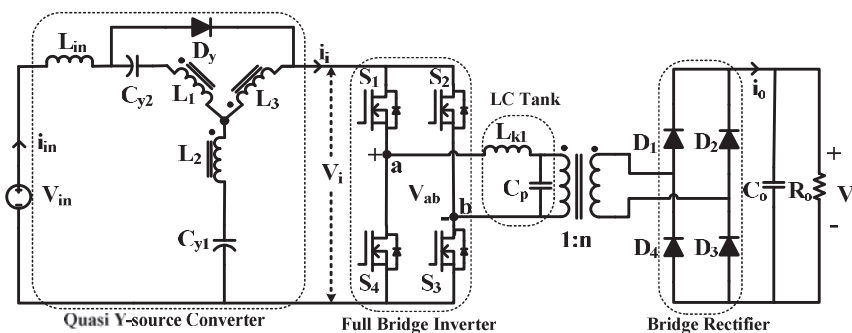
The first isolated impedance source DC/DC converter was introduced in 2009 [20]. It inherits all the features of the conventional Z-source network. In [21], the reliability and efficiency are improved with a reduced number of switches. However, these converter's DIC nature is not recommended for PV and fuel cell applications. To resolve this issue, researchers are introduced a CIC isolated quasi-Z source DC/DC converter [22, 23]. Hence, the CIC feature of these converters is mainly preferred for renewable energy resources. Furthermore, magnetically coupled ISC are presented in [24, 25] to improve the gain. The converter in [24], gain is improved by coupled inductor and isolation transformer with reduced switch count. Moreover, due to the DIC nature, this converter is not preferred. In [25], researchers developed a magnetically coupled CIC Y-source DC/DC converter. Moreover, all aforementioned converters are hard switched converters so that turn-on and turn-off losses are more and impact on the overall converter efficiency. Researchers are made efforts to develop soft switching in impedance source DC/DC converters [26–28]. However, the converters in [26, 27] are soft switched and high gain these are not preferred due to non-isolated type. In [28] soft switched, isolated high gain ISC is presented with computerized simulation.

This paper's main objective is to design high efficiency, compact size, low voltage stress on semiconductor devices and higher power density DC/DC converter to interface renewable energy resources. In the literature, the soft switched frequency modulated high gain DC/DC impedance source converters are not extensively investigated. In this paper, authors are made efforts to develop soft switched frequency modulated impedance source DC/DC converters. To obtain higher gain a magnetically coupled three winding coupled inductor and high frequency transformer is used. Here, output

voltage is regulated by varying the switching frequency. Furthermore, soft switching (ZCS) is obtained by properly selecting LC tank, which causes the partial resonance during shoot through instant, and all the active devices (MOSFETs) are turned off with ZCS. There are no additional magnetic components, active and passive devices are used for achieving soft switching (ZCS). This improves the overall efficiency of the converter. Since converter having soft switching feature high frequency operation is possible. Hence magnetic component and other filter capacitor size can be reduced which enhance the power density. Also due to ZCS, the turn off voltage spikes on switches (which is typical problem in current fed converters) are eliminated. This converter inherits all the features of ISC, and it overcome the demerits of a conventional converter [13]. In Section 2 steady state operation and description of the proposed converter is discussed. The design analysis, simulation and experimental results are presented in Sections 3 and 4.

## 2 Discription and Operation of the Proposed Converter

In Figure 1, the proposed isolated quasi-Y source DC/DC converter is shown. This converter consists of three winding coupled inductors ( $L_1$ ,  $L_2$ , and  $L_3$ ) having  $N_1$ ,  $N_2$ , and  $N_3$  number of turns in the respective windings, two capacitors  $C_{y1}$ ,  $C_{y2}$ , input inductor  $L_{in}$  and diode  $D_y$ . The two DC blocking capacitors  $C_{y1}$  and  $C_{y2}$  are used to prevent core saturation in the Y-source coupled inductor. The input inductor is connected in series with the voltage source, and the blocking diode  $D_y$  is connected between the drain of the active switch and the negative terminal of the capacitor  $C_{y2}$ . The output of the quasi-Y source converter is connected to the bridge inverter. The primary and secondary sides of the isolated high-frequency transformer (HFT) are



**Figure 1** Proposed isolated quasi-Y source DC/DC converter.

connected to the inverter and rectifier bridges. Here, the LC tank is formed by utilizing the transformer's parasitic like leakage inductance ( $L_{k1}$ ) and winding capacitor ( $C_p$  parasitic capacitor). However, partial resonance is obtained by proper selection of LC tank. This allows all switches in the inverter will turn off with ZCS. The output voltage is controlled using the frequency modulation technique while maintaining the shoot-through duty ratio ( $d_{ST}$ ) constant. Here, to utilize the CIC and extensive features of the impedance network presented in [18] is taken. Moreover, the converter in [18] is a non-isolated, PWM-controlled, and hard switched converter. Here, efforts are made to develop a soft switched isolated and frequency modulated high gain converter for renewable energy applications.

## 2.1 Configuration of Quasi-Y Source Topology [18]

Figure 2(a) presents the equivalent circuit of the CIC quasi-Y source converter. It has three coupled inductors ( $L_1, L_2,$  and  $L_3$ ), one input inductor  $L_{in}$ , one blocking diode  $D_y$ , two dc capacitors  $C_{y1}, C_{y2}$ , and one active switch  $S_{sw}$ . Here,  $L_m$  is the magnetizing inductance of the Y-source coupled inductor with respect to winding one, and  $V_L$  is the voltage across this winding 1.  $N_1, N_2,$  and  $N_3$  are the number of turns in each winding. From Figure 2(b), (c), this converter mainly operates in shoot-through and non-shoot through states respectively.

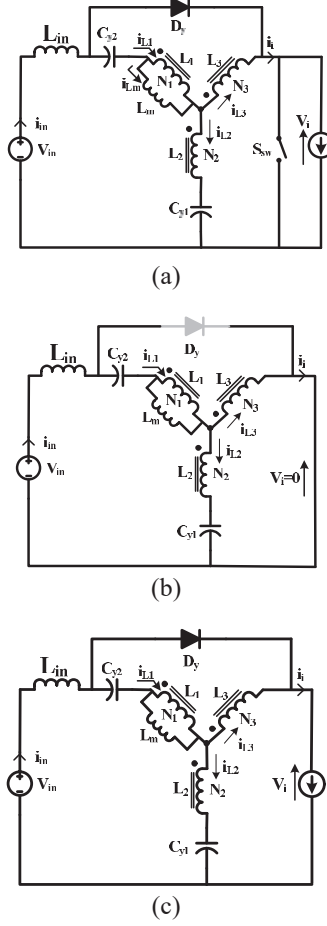
The shoot-through state is depicted in Figure 2(b), in this state, active switch  $S_{sw}$  is conducting, and diode  $D_y$  is OFF. During this state, input inductor  $L_{in}$  and magnetizing inductor  $L_m$  are charged. By analysing the circuit, the steady-state analysis can obtain as follows.

$$-V_{C_{y1}} - n_{21}V_L + n_{31}V_L = 0; V_L = \frac{V_{C_{y1}}}{(n_{31} - n_{21})} \quad (1)$$

$$\begin{aligned} -V_{in} + V_{L_{in}} - V_{C_{y2}} + V_L + n_{21}V_L + V_{C_{y1}} &= 0 \\ V_{L_{in}} &= V_{in} + V_{C_{y2}} - V_{C_{y1}} - (1 + n_{21})V_L \end{aligned} \quad (2)$$

Non-shoot through state is presented in Figure 2(c). During this state, switch  $S_{sw}$  is OFF, and diode  $D_y$  is conducting. By analysing the circuit, the following expressions are obtained.

$$V_{C_{y2}} - n_{31}V_L - V_L = 0; V_L = \frac{V_{C_{y2}}}{(n_{31} + 1)} \quad (3)$$



**Figure 2** Equivalent circuit (a) CIC quasi-Y source converter, (b) Shoot through state, (c) Non-shoot through state.

$$-V_{in} + V_{L_{in}} - V_{C_{y2}} + V_L + n_{21}V_L + V_{C_{y1}} = 0$$

$$V_{L_{in}} = V_{in} + V_{C_{y2}} - V_{C_{y1}} - (1 + n_{21})V_L \quad (4)$$

$$-V_{in} + V_{L_{in}} + V_i = 0; V_i = V_{in} - V_{L_{in}} \quad (5)$$

$$V_i = V_{C_{y1}} - V_{C_{y2}} + (1 + n_{21})V_L \quad (6)$$

Here,  $n_{21} = \frac{N_2}{N_1}$ ,  $n_{31} = \frac{N_3}{N_1}$  are turns ratios of  $N_1, N_2, N_3$  and  $V_i$  is the DC link voltage.

By state-space averaging, from (1) and (3) the resultant can obtain as follows.

$$\begin{aligned} \frac{V_{C_{y1}}}{(n_{31} - n_{21})} d_{ST} + \frac{V_{C_{y2}}}{(n_{31} + 1)} (1 - d_{ST}) &= 0 \\ \frac{V_{C_{y2}}}{V_{C_{y1}}} &= \frac{(n_{31} + 1) d_{ST}}{(n_{31} - n_{21})(1 - d_{ST})} \end{aligned} \quad (7)$$

Applying state-space averaging at input inductor  $L_{in}$ , by using (2), (4) and after solving the below equation, we will obtain (8).

$$\begin{aligned} \{V_{in} + V_{C_{y2}} - V_{C_{y1}} - (1 + n_{21})V_L\} d_{ST} \\ + \{V_{in} + V_{C_{y2}} - V_{C_{y1}} - (1 + n_{21})V_L\} (1 - d_{ST}) &= 0; \\ V_{C_{y2}} &= V_{C_{y1}} - V_{in} \end{aligned} \quad (8)$$

By using (7) and (8), the simplified individual capacitor voltages are obtained as

$$V_{C_{y1}} = \frac{(1 - d_{ST})V_{in}}{1 - \left(\frac{n_{21}+1}{n_{21}-n_{31}}\right) d_{ST}} \quad (9)$$

$$V_{C_{y2}} = \frac{\left(\frac{n_{31}+1}{n_{21}-n_{31}}\right) d_{ST} V_{in}}{1 - \left(\frac{n_{21}+1}{n_{21}-n_{31}}\right) d_{ST}} \quad (10)$$

By substituting (3), (9), and (10) in (6), the resultant DC link voltage can be obtained as follows.

$$V_i = \frac{1}{1 - \left(\frac{1+n_{21}}{n_{21}-n_{31}}\right) d_{ST}} V_{in} = \frac{1}{(1 - \delta d_{ST})} V_{in} \quad (11)$$

Here,  $\delta$  is the winding factor of quasi-Y source coupled inductor.

$$\delta = \frac{1 + n_{21}}{n_{21} - n_{31}} = \frac{N_1 + N_2}{N_2 - N_3}, \quad \text{and} \quad n_{21} = \frac{N_2}{N_1}, \quad n_{31} = \frac{N_3}{N_1}. \quad (12)$$

For each selected value of  $\delta$ , various combinations of turns ratios  $N_1 : N_2 : N_3$  are realized, illustrated in the Table 1.

From Equation (11), the allowable shoot through duty variation is given as follows

$$0 \leq d_{ST} \leq d_{ST,max} = \frac{1}{\delta} \quad (13)$$

**Table 1** Realization of Shoot-through duty ratio ( $d_{ST}$ ) and winding factor ( $\delta$ ) with different turns ratios ( $N_1: N_2: N_3$ )

$\delta = \frac{N_1 + N_2}{N_2 - N_3}$	$d_{ST,max}$	Conventional Duty Range (D)	( $N_1: N_2: N_3$ ) Turns Ratio
2	1/2	$0.5 \leq D \leq 3/4$	(1:3:1), (2:4:1), (3:5:1)
3	1/3	$0.5 \leq D \leq 4/6$	(1:4:1), (3:3:1), (2:4:2)
4	1/4	$0.5 \leq D \leq 5/8$	(2:2:1), (1:3:2), (5:3:1)
5	1/5	$0.5 \leq D \leq 6/10$	(3:2:1), (2:3:2), (1:4:3)
6	1/6	$0.5 \leq D \leq 7/12$	(4:2:1), (3:3:2), (2:4:3)
7	1/7	$0.5 \leq D \leq 8/14$	(4:3:2), (5:2:1), (3:4:3)
8	1/8	$0.5 \leq D \leq 9/16$	(5:3:2), (6:2:1), (3:5:4)

The relation of  $d_{ST}$  and conventional duty (D) is given as below.

$$d_{ST} = 2D - 1 \quad (14)$$

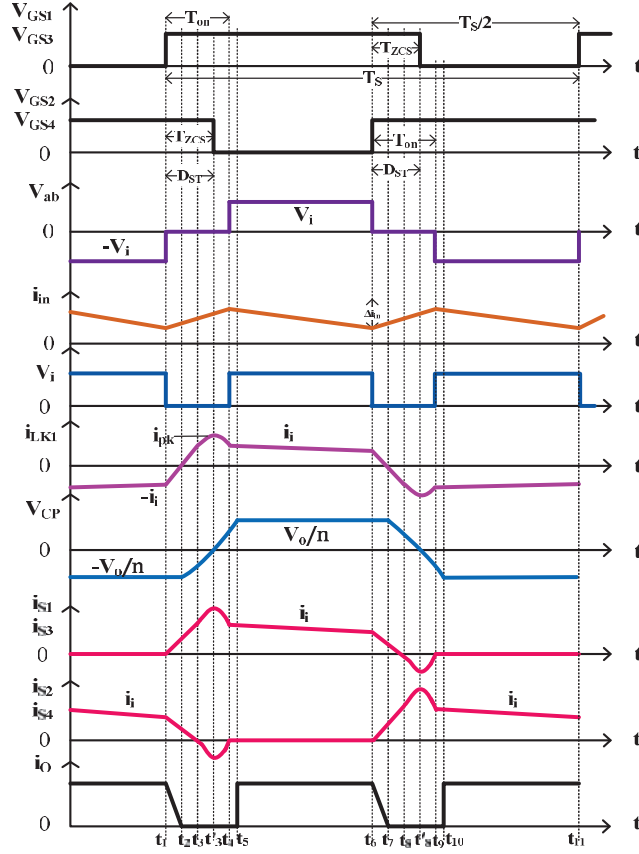
## 2.2 Steady State Analysis and Modes of Operation of the Proposed Converter

The steady-state waveform of the proposed converter is presented in Figure 3. Here, by utilizing the transformer's parasitic  $L_{k1}$  and  $C_p$ , soft switching (ZCS) is achieved at the turn-off instant. To regulate the output voltage, here frequency modulation technique is implemented. Here constant shoot through duty ( $d_{ST}$ ) is chosen for soft computation of power MOSFETs. The gate signals, pair of  $V_{GS1}$ ,  $V_{GS3}$ , and pair of  $V_{GS2}$ ,  $V_{GS4}$  is  $180^\circ$  phase-modulated each other with small  $D_{ST}$ . The converter analysis is studied for the first half cycle over five operating modes with detailed discussion is given. The equivalent circuit operation is depicted in Figure 4.

### Mode I: $t_1 \sim t_2$ [Figure 4(a)]

This mode is started at  $t_1$ . Before that, power MOSFETs  $S_2$ ,  $S_4$  are in conduction, and energy is transferred from source to load. At  $t = t_1$ , the MOSFET pairs  $S_1$  and  $S_3$  are triggered, and all the MOSFETs are under conduction. In a bridge rectifier,  $D_2$  and  $D_4$  are conducting, and  $D_1$  and  $D_3$  are off. The diode  $D_y$  in the impedance network is also off. Here, the leakage inductor  $L_{k1}$  and input inductor  $L_{in}$  starts charging. The current flows through  $L_{k1}$  and  $L_{in}$  linearly increases. The current through the power MOSFETs  $S_1$ ,  $S_3$  increases, whereas in  $S_2$ ,  $S_4$  are decreased, and these can be observed in





**Figure 3** The steady-state waveforms of the quasi-Y source DC/DC impedance converter.

Figure 3. The voltage across  $C_p$  and current through  $L_{k1}$  is given as follows.

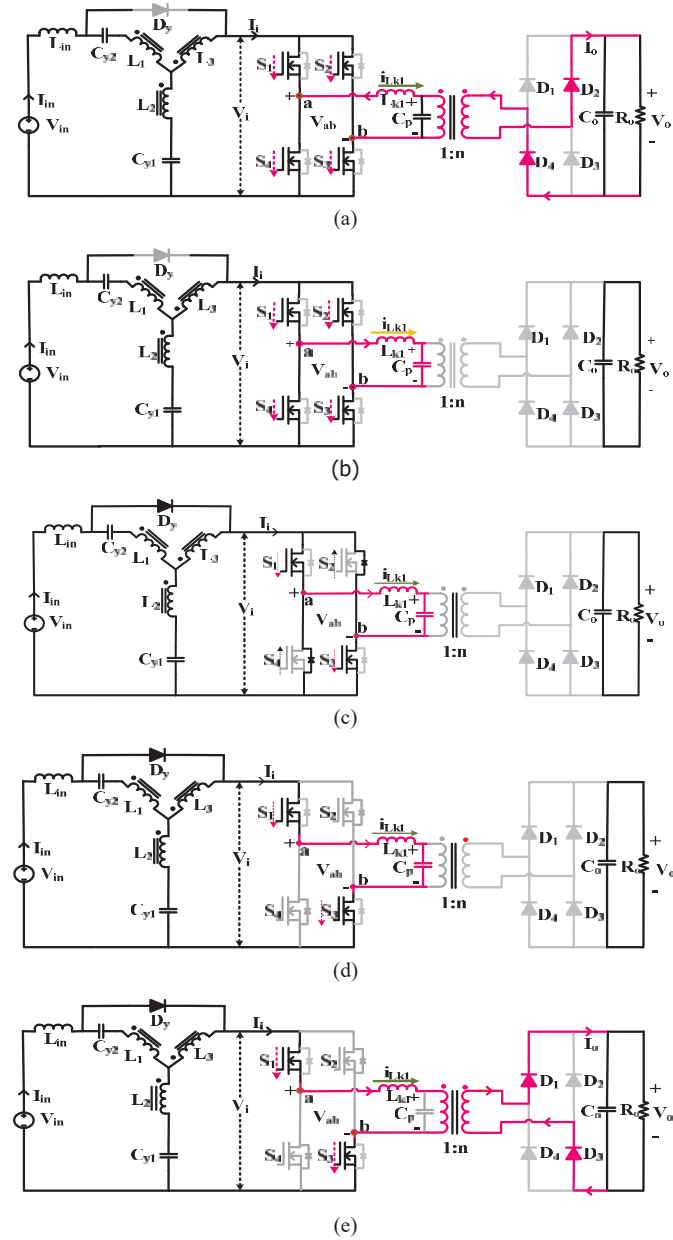
$$V_{C_p}(t) = -\frac{1}{n}V_O \quad (15)$$

$$i_{L_{k1}}(t) = \frac{V_O}{nL_{k1}}(t - t_1) - I_i \quad (16)$$

Time duration for this Mode I is obtained as follows

$$T_{21} = t_2 - t_1 = \frac{nI_iL_{K1}}{V_O} \quad (17)$$

Here  $n$  is the turns ratio of HFT, and this mode ends at  $t_2$  when  $L_{k1}$  current reaches zero.



**Figure 4** Operating modes of proposed topology (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V.

**Mode II:  $t_2 \sim t_3$  [Figure 4(b)]**

This mode will start at  $t_2$ , when diodes  $D_2, D_4$  in the bridge rectifier are reverse biased. All the power MOSFETs are conducting, and  $D_y$  is off. The transformer's parasitic  $L_{k1}$  and  $C_p$  form the LC tank cause resonance in the circuit. The current through switch pairs  $S_1$  and  $S_3$  is still increasing, and the switch pairs  $S_2$  and  $S_4$  are decreasing.

The current through  $L_{k1}$  is given as

$$i_{L_{k1}}(t) = \frac{V_O}{nZ_r} \sin(w_r(t - t_2)) \quad (18)$$

$$w_r = 2\pi f_r, f_r = \frac{1}{2\pi\sqrt{L_{k1}C_p}} \quad (19)$$

$$Z_{cr} = \sqrt{\frac{L_{k1}}{C_p}} \quad (20)$$

Here,  $z_{cr}$ ,  $f_r$ , and  $w_r$  are characteristic impedance of the network, resonant frequency, and angular frequency respectively. The time duration for this mode is given in (21)

$$T_{32} = t_3 - t_2 = \frac{1}{W_r} \sin^{-1} \left( \frac{nI_i Z_{cr}}{V_O} \right), 0 < w_r T_{32} < \frac{\pi}{2} \quad (21)$$

**Mode III:  $t_3 \sim t_4$  [Figure 4(c)]**

This mode will start at  $t_3$  when the value of leakage inductor current  $i_{L_{k1}}$  is equal to  $I_i$ . At this instant, the current through the power MOSFETs  $S_2, S_4$  is zero and which are turned off with ZCS. Currently, the conducting devices are  $S_1, S_3$ , body diodes of  $S_2, S_4$ , and  $D_y$ . The current through  $L_{k1}$  reaches the peak value  $I_{pk}$  at  $t = t'_3$ , whereas voltage across the  $C_p$  is zero.

$$I_{Pk} = \frac{V_O}{nZ_{cr}} \geq I_i \quad (22)$$

Here  $I_{pk}$  is the peak value of  $L_{k1}$  current, and the time duration ( $t_4 - t_2$ ) is given by

$$T_{42} = \frac{\pi - w_r T_{32}}{w_r} \quad (23)$$

**Mode IV:  $t_4 \sim t_5$  [Figure 4(d)]**

At  $t = t_4$ , when the  $L_{k1}$  current ( $i_{L_{k1}}$ ) reaches to  $I_i$  this mode will start. This instant body diodes of  $S_2, S_4$  turned off, and the power MOSFETs  $S_1, S_3$ ,

diode  $D_y$  are still conducting. Here at the end of this mode parasitic capacitor  $C_p$  is fully charged with  $I_i$  current. The time taken for this mode is given as follows

$$T_{54} = t_5 - t_4 = \frac{V_O(1 + \cos(w_r(t_4 - t_2)))C_P}{nI_i} \quad (24)$$

### Mode V: $t_5 \sim t_6$ [Figure 4(e)]

During this mode,  $C_p$  is fully charged with voltage of  $V_i$  and the diodes  $D_1$ ,  $D_3$  in rectifier bridge start conducting. Here, the power MOSFETs  $S_1$ ,  $S_3$  and  $D_y$  are in conduction. Here energy is transferring to the load and leakage inductor current  $i_{L_{K1}}(t)$  is equal to the  $I_i$ .

$$i_{L_{K1}}(t) = I_i \quad (25)$$

The time duration for half switching period ( $T_s/2$ ) is equal to total time duration of Mode I to V, and it is given as follows

$$t_6 - t_1 = \frac{1}{2}T_s \quad (26)$$

## 3 Design Analysis of the Quasi-Y Source Converter

In the CIC quasi-Y source converter, the coupled inductor is represented by a three-winding ideal transformer with leakage inductance and magnetizing inductance of each winding. Here all the power MOSFETs and diodes are ideal.

### 3.1 Voltage Gain (M)

The average output current ( $I_{R_o}$ ) is given as

$$I_{R_o} = \frac{V_o}{R_o} = \frac{I_{L_{k1, avg}}}{n} = \frac{2}{nT_s} \int_0^{\frac{T_s}{2}} I_{L_{k1}}(t) dt \quad (27)$$

From the power balance equation

$$P_o = \frac{V_o^2}{R_o} = \eta V_{in} I_{in} = \eta V_i I_i \quad (28)$$

$$I_i = \frac{V_o^2}{\eta V_i R_o} \quad (29)$$

Here  $\eta$  is the efficiency of the converter,  $n$  is the turns ratio of the HFT, and  $R_o$  is the full load resistance.

By using (26), (27), and (29), the voltage at the output side is obtained as

$$V_o = \frac{n\eta V_i}{1 - 2f_s \left( \frac{1}{2}T_{21} + T_{42} + T_{54} \right)} \quad (30)$$

The output voltage can be obtained by substituting the Equations (17), (23), and (25) in (30). Hence it is derived as follows.

$$V_o = \frac{n\eta V_i}{1 - f_n \left( 1 + \frac{x}{2\pi} - \frac{1}{\pi} \sin^{-1} x + \frac{1}{\pi} \frac{(1-\sqrt{1-x^2})}{x} \right)} \quad (31)$$

The proposed converter gain is obtained as

$$M = \frac{V_o}{V_{in}} = \frac{V_o}{V_i} * \frac{V_i}{V_{in}} \quad (32)$$

By using (11), (31), and (32) the resultant gain of the proposed converter is obtained as

$$M = \frac{V_o}{V_{in}} = \frac{n\eta}{1 - f_n \left( 1 + \frac{x}{2\pi} - \frac{1}{\pi} \sin^{-1} x + \frac{1}{\pi} \frac{(1-\sqrt{1-x^2})}{x} \right)} \times \frac{1}{(1 - \delta d_{ST})} \quad (33)$$

Here,  $f_n = \frac{f_s}{f_r}$ ,  $x = \frac{M}{n\eta r_n}$ ,  $r_n = \frac{1}{n^2} \times \frac{R_o}{Z_r}$ ,  $f_n$  = Normalized frequency,  $f_s$  = Switching frequency,  $f_r$  = Resonant frequency,  $M$  = Gain of the converter,  $r_n$  = Normalized resistance,  $R_o$  = Full load output resistance,  $Z_r$  = Characteristic impedance. The gain of the converter for the ideal case depends on the turns ratio of the transformer ( $n$ ), winding factor (12), and shoot through duty ( $d_{ST}$ ). The gain of the proposed converter is shown in Figure 5 at different turns ratio of the transformer. The converter gain is increased by increasing the turns ratio of the transformer.

### 3.2 Design of Input Inductor

The input inductor can be designed based on the current ripple. The current ripple at the input inductor is given as

$$\Delta I_{L_{in}} = \int_{d_{ST}T_s}^{T_s} \frac{di_{L_{in}}}{dt} dt = \int_{d_{ST}T_s}^{T_s} \frac{V_{L_{in}}}{L_{in}} dt = \frac{V_{L_{in}}}{L_{in}} (1 - d_{ST}) T_s \quad (34)$$

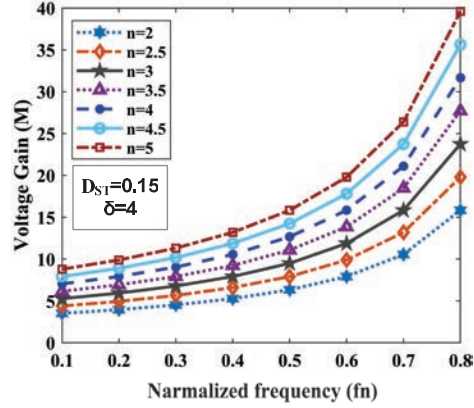


Figure 5 Gain curve with normalized frequency ( $f_n$ ).

From Equation (5)

$$V_{L_{in}} = V_{in} - V_i \tag{35}$$

$$L_{in} = \frac{(V_{in} - V_i)(1 - d_{ST})}{\Delta I_{L_{in}} f_s} \tag{36}$$

### 3.3 Condition for ZCS

Here the LC tank must be designed properly to obtain ZCS. The  $L_{k1}$  and  $C_p$  stored energy is mainly responsible for achieving soft switching, and selected value  $Z_{cr}$  should satisfy the following condition.

$$Z_{cr} < \frac{V_0}{nI_{i,max}} = \frac{V_{in,min}R_o}{nV_O} \tag{37}$$

### 3.4 $L_{k1}$ and $C_p$ Design

The transformer parasitic's  $L_{k1}$  and  $C_p$  must be chosen carefully to accomplish ZCS. The characteristic impedance ( $Z_{cr}$ ) is obtained from Equation (37). By utilizing Equations (20) and (37), the  $L_{k1}$ ,  $C_p$  parameters are calculated. The selected value of  $Z_{cr}$  should satisfy the ZCS condition (37).

### 3.5 Voltage Stress of MOSFETs and Diodes

The voltage stress on MOSFETs and output diodes is given in (37), (38). From (37), the voltage stress on all MOSFETs is dependent on the output

voltage and the number of turns in the HFT. The diodes voltage stress is the same as the output voltage.

$$V_{S_{1-4}} = \frac{V_o}{n} = V_i \tag{38}$$

$$V_{D_{1-4}} = V_o \tag{39}$$

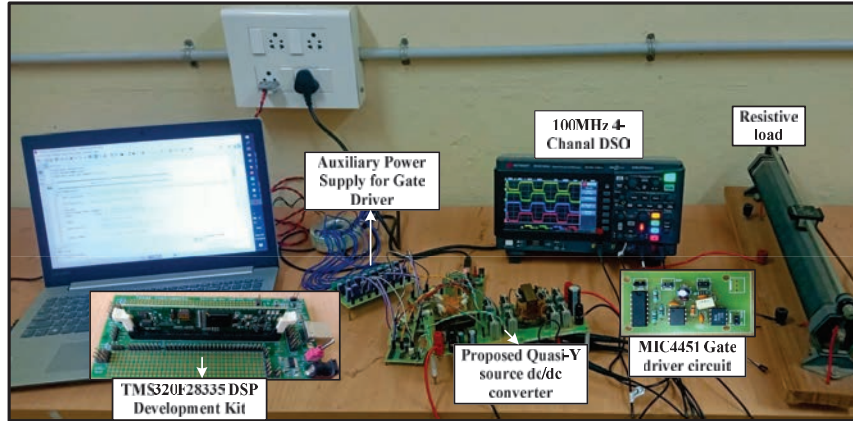
#### 4 Discussion on Simulation/Hardware Results

The performance of a quasi-Y source high gain DC/DC resonant converter using PSIM Simulink, and hardware prototype is presented. Here, the converter is designed for 300 W power and, the input voltage varies (40–60) V and output is regulated to standard 380 V DC grid voltage. Here output voltage is regulated by varying switching frequency at constant shoot through duty ( $d_{ST}$ ). The switching frequency is varied from 85 kHz to 190 kHz. When the input voltage is 40 V, to regulate the rated output voltage converter is operated at 190 kHz and when input voltage is 60 V to regulate the rated output an 85 kHz switching frequency is applied. In Table 2, the converter specifications and other design parameters are given.

The experimental photograph of the converter is shown in Figure 6. The coupled inductor is designed using EE55 gapped ferrite core with a 16:16:8 number of turns. All the windings are wound tightly in Y shape manner. EE42

**Table 2** Components and parameters specifications

Parameter	Specification Value
Rated Power ( $P_o$ )	300 W
Input voltage ( $V_{in}$ )	40–60 V
Output voltage ( $V_o$ )	380 V
Switching frequency ( $f_s$ )	85–190 kHz
Shoot through duty ( $d_{ST}$ )	0.15
Input inductor ( $L_{in}$ )	2 mH
Capacitors	$C_{y1} = 68 \mu\text{F}$ , $C_{y2} = 22 \mu\text{F}$ , $C_o = 200 \mu\text{F}$
Power MOSFETs	IRFP4227pbf, $R_{DS(on)} = 21 \text{ m}\Omega$
Diodes	RHRG75120
Coupled Inductor ( $N_1 : N_2 : N_3$ )	EE55/28/21 Ferrite core (16:16:8)
Winding Factor ( $\delta$ )	4
HFT ( $N_1 : N_2$ )	EE42/21/15 Ferrite core (4: 20)
$L_{k1}$	0.85 $\mu\text{H}$
$C_p$	0.18 $\mu\text{F}$



**Figure 6** Experimental prototype of Quasi-Y source DC/DC converter.

ferrite core is used for HFT. Hence, the tight coupling of the inductor and transformer results in less parasitic resistance and leakage in each winding. Moreover, to reduce the skin effect and ac resistance of winding Litz wires are used. For generating gate signals, (TMS320F28335) TI supported C2000 development kit is used. All the active and passive components are selected to achieve lower losses.

The simulation and experimental tests are performed at rated power of 300 W with 48 V input voltage. The output voltage is regulated to 380 V by varying the switching frequency up to 150 kHz. The switching pulses of the proposed topology with small shoot-through duty ( $d_{ST} = 0.15$ ) presented in a dotted circle and operating at 150kHz switching frequency are shown in Figure 7. Here, the gate pulse of MOSFETs 1, 3, and MOSFETs 2, 4 are modulated with a  $180^\circ$  phase difference.

The key waveforms of simulation results are shown in Figures 8(a), 9(a), 10(a), 11(a), respectively. The developed prototype experimental results are shown in Figures 8(b), 9(b), 10(b), 11(b). Here, the simulation and experimental test are done at the rated condition of the developed converter. Both simulated and experimental results are found to be identical.

Figure 8 shows simulation and hardware results of gate signal ( $V_{gs1}$ ,  $V_{gs3}$ ), voltage stress ( $V_{ds1}$ ,  $V_{ds3}$ ), and currents ( $I_{S1}$ ,  $I_{S3}$ ) through the active switch pairs  $S_1$ ,  $S_3$ . The simulation and experimental results of gate signal ( $V_{gs2}$ ,  $V_{gs4}$ ), voltage stress ( $V_{ds2}$ ,  $V_{ds4}$ ), and currents ( $I_{S2}$ ,  $I_{S4}$ ) through the switch pairs  $S_2$ ,  $S_4$  are depicted in Figure 9. It is observed from Figures 8, 9 all the switches  $S_1$  to  $S_4$  are turned off with ZCS and denoted in a dotted



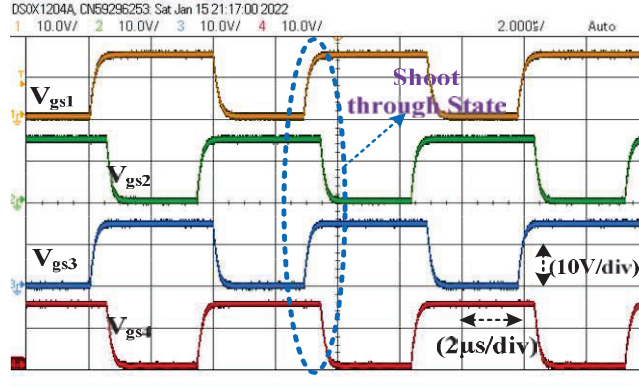


Figure 7 Gate pulse of the proposed converter at switching frequency  $f_s = 150$  kHz.

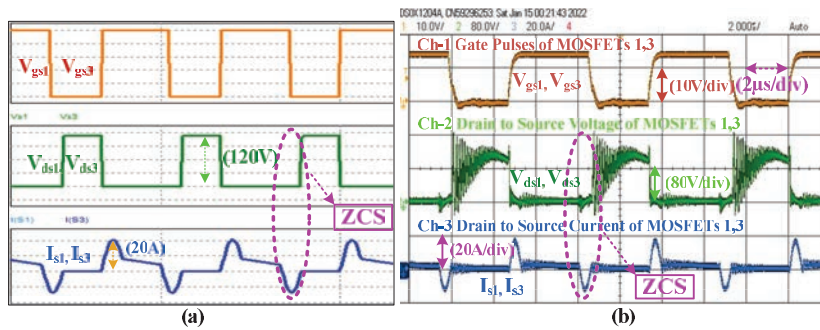


Figure 8 Standard waveforms obtained from (a) simulation and (b) Experimental results of gate signals, voltage stress, current through the pair of switches  $S_1, S_3$  at rated condition.

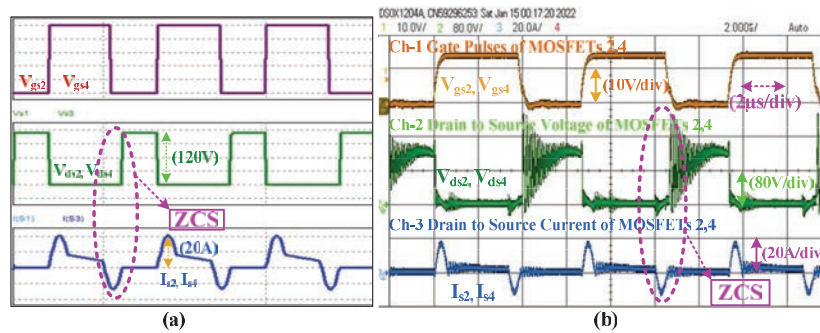
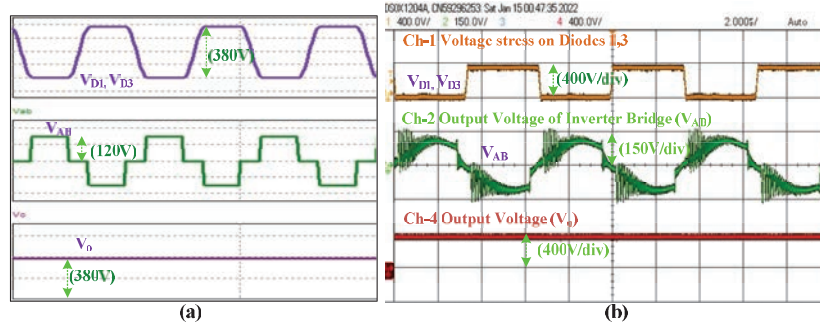
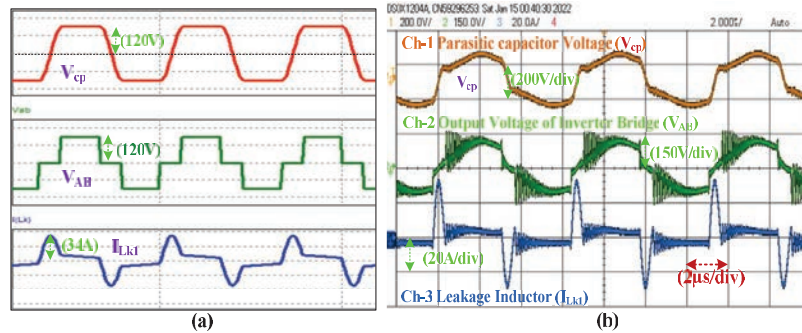


Figure 9 Standard waveforms obtained from (a) simulation and (b) Experimental results of gate signals, voltage stress, current through the pair of switches  $S_2, S_4$  at rated condition.



**Figure 10** Standard waveforms obtained from (a) simulation and (b) Experimental results of diode voltage ( $V_{D1}$ ,  $V_{D3}$ ), inverter output ( $V_{ab}$ ), output voltage ( $V_o$ ) at rated condition.



**Figure 11** Standard waveforms obtained from (a) simulation and (b) Experimental results of parasitic capacitor voltage ( $V_{Cp}$ ), inverter output voltage ( $V_{ab}$ ), Current through Leakage inductor ( $I_{Lk1}$ ) at rated condition.

circle. It helps the converter can operate at a higher frequency with lower switching losses. The voltage of the switches is settled at 120 V, and the peak current reaches 20 A during the shoot-through instant.

Figure 10 shows the simulation and experimental results of voltage stress on rectifier diodes ( $V_{D1}$ ,  $V_{D3}$ ), output of inverter bridge voltage ( $V_{AB}$ ) and output voltage ( $V_o$ ). The simulation and experimental results have observed that peak value of diode and output voltage is settled at 380 V. At the same time, the inverter output voltage ( $V_{AB}$ ) is settled at 120 V. In Figure 11, the voltage across the parasitic capacitor ( $V_{Cp}$ ), the output of inverter bridge voltage ( $V_{AB}$ ) and current through the leakage inductor ( $I_{Lk1}$ ) are shown. The simulation and experimental results were observed that parasitic and inverter bridge voltage is settled at 120 V. When  $I_{Lk1}$  reaches a peak value of 36 A, the same instant  $V_{Cp}$  voltage is zero.

**Table 3** Losses equations used to compute losses in the converter

Description	Equation
Gate driver losses	$C_{iss} \times V_g^2 \times f_{sw}$
Capacitor losses	$I_{Co,rms}^2 \times R_{ESR}$
Switch conduction losses	$I_{sw,rms}^2 \times R_{DS(on)}$
Turn on losses in the switch	$\frac{1}{2} C_{oss} \times V_{sw}^2 \times f_{sw}$
Total losses in rectifier diodes	$V_{Df} I_{D,avg} + I_{D,rms}^2 R_D + V_d Q_{rr} f_{sw}$
Total losses in the HFT	$I_{t,rms}^2 R_{winding} + P_c \text{ limit } V_e$
Total losses in the inductor	$I_{L,rms}^2 R_{L,DC} + P_c \text{ limit } V_e$

**Table 4** Efficiency calculations of proposed converter

Input Voltage	Parameter	50 W	150 W	300 W
40 V	Po	47.425	145.642	290.92
	Losses	1.513	4.137	9.104
	Efficiency	96.9	97.23	96.96
48V	Po	47.613	147.243	291.83
	Losses	1.271	3.112	7.021
	Efficiency	97.39	97.93	97.65
60V	Po	48.512	147.431	292.967
	Losses	1.005	2.425	6.192
	Efficiency	97.97	98.38	97.93

The individual losses in each element are computed by using loss equations given in Table 3 and the parameters of selected components in the datasheet. The efficiency of the converter is obtained by using Equation (40) and associated total losses in the converter. Here, some of the efficiency model calculations are tabulated in Table 4.

$$\text{Efficiency } (\eta) = \frac{P_o}{P_o + \text{losses}} \times 100 \quad (40)$$

Were

$C_{iss}$  = Switch input capacitor (F)

$V_g$  = Switch driving voltage (V)

$f_{sw}$  = Switching frequency (Hz)

$I_{Co,rms}$  = Capacitor rms ripple current (A)

$R_{ESR}$  = Capacitor equivalent series resistor ( $\Omega$ )

$I_{sw,rms}$  = Switch rms current (A)

$R_{DS(on)}$  = Switch drain to source on-state resistance ( $\Omega$ )

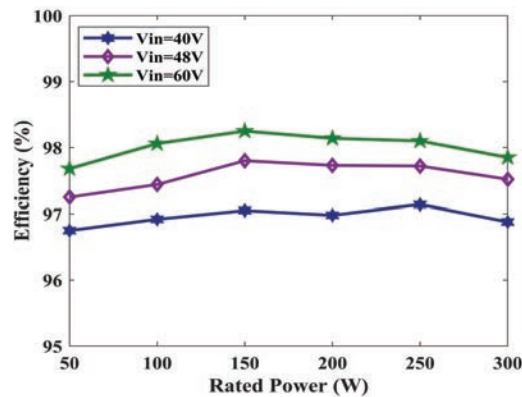
$C_{oss}$  = Switch output capacitor (F)

- $V_{sw}$  = Switch average voltage at turn off time (V)  
 $V_{Df}$  = Diode forward voltage (V)  
 $I_{D,rms}$  = Diode rms current (A)  
 $I_{D,avg}$  = Diode average current (A)  
 $R_D$  = Diode turn on resistance ( $\Omega$ )  
 $V_d$  = Diode blocking voltage (V)  
 $Q_{rr}$  = Diode reverse recovery charge  
 $I_{t,rms}$  = rms current through transformer (A)  
 $R_{winding}$  = Transformer DC resistance ( $\Omega$ )  
 $P_{C\ limit}$  = Core loss limit ( $mW/cm^3$ )  
 $V_e$  = Effective core volume ( $cm^3$ )  
 $I_{t,rms}$  = rms current through transformer (A)

At 60 V rated power (300 W) the calculated efficiency of the converter is given below.

$$\begin{aligned}
 \text{Efficiency } (\eta) &= \frac{P_o}{P_o + \text{losses}} \times 100 \\
 &= \frac{292.967}{292.967 + 6.192} \times 100 = 97.93\%
 \end{aligned}$$

The mathematical efficiency calculation of converter is given in Table 4. The maximum efficiency of 98.38% is obtained for 60 V input at 150 W power. Minimum efficiency of 96.90% for 40 V input with 50 W power. In Figure 12 the measured efficiency of the converter is given. Here, the experimental efficiency values are slightly lesser then the mathematically



**Figure 12** Efficiency of the proposed converter.

calculated one. But both are very close, and the slight variation is due to the change in the resistance of the semiconductor while operating temperature changes.

## 5 Conclusion

A quasi-Y source magnetically coupled isolated partial resonant DC/DC converter is presented. By utilizing HFT parasitic components, LC parallel tank is formed, and soft switching (ZCS) occurs during the MOSFET turn-off instant. The mathematical and design methodology of the proposed converter is discussed. In addition, the simulation and experimental results are used to analyze the performance of the converter. Furthermore, coupled inductor and HFT provide a high voltage gain with less voltage stress on MOSFETs. Furthermore, it brings merits of ISC, and the soft switching feature improves the converter efficiency up to 98.38% at 60 V input voltage. The high gain, galvanic isolation and CIC feature of this converter are most suitable for renewable energy applications.

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