
Protection Algorithm for Fault Identification and Isolation in DC Microgrid

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Abstract

In renewable energy dominated distributed ring configuration direct current (DC) networks, the protection philosophy is one of the critical challenging task. It is due to the existence of power electronic converters and erratic attributes of distributed energy sources. Consequently, conventional current direction based as well as over current protection strategies is not applicable for DC microgrids. In this paper, protection algorithm for fault recognition and isolation of faulty line is presented based on the polarity of change in inductance immediately after fault inception. The voltage and current sample information is used to determine the parameter by employing the least square estimation (LSE) technique. The efficiency of the proposed method is tested for internal and external faults, the impact of fault resistance and fault location, different system configurations, and load change conditions in MATLAB/Simulink simulation. It is noted that proposed method would categorize internal and external faults perfectly. The operating time of the proposed protection method is comparatively less than the existing methods.

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It also improves selectivity, security, and reliability under above mentioned abnormal cases.

Keywords: Fault recognition, DC microgrid protection, fault isolation, protection devices, and polarity of change in inductance.

1 Introduction

Nowadays, the rise in power demand along with environmental conditions attracts researchers to enhance the performance of existing power networks. The penetration of nonconventional energy sources maintains an uninterrupted power supply to the consumers and also assists in developing a contamination free environment [1, 2]. The spread of DC loads will strengthen the development of a direct current (DC) microgrid rather than an alternate current (AC) microgrid [3]. The DC microgrid holds many advantages as compared to the AC microgrid such as, the absence of skin effect, increase in overall system efficiency, reduction in power conversion stages, simplified converter control strategies, no synchronization issue due to the absence of frequency and reactive power [4, 5]. Nevertheless, the DC system demands sophisticated protection philosophy due to the involvement of power converters [6]. A protection system should ensure the enhancement of reliability, dependability, and selectivity of the system [7]. In the DC grid, the converters limit the fault current value due to current limiting nature, and this limited fault current may be similar to the disturbance due to load change [8]. Hence, the recognition of DC faults is more complicated by implementing an overcurrent protection method [9]. The fault resistance and location changes will impact the current magnitude [10]. [11] has presented an overcurrent protection scheme that identifies appropriate fault segments during low fault resistance values. Nevertheless, this current based scheme may not be accurate during high resistance faults. [12], introduced the current difference based protection technique for low voltage DC grid. However, its performance is not efficient during low current magnitude faults. In [13] have detailed about the current differential protection approach for DC ring configuration microgrid. However, it needs a dedicated communication arrangement to transfer the data from one end to another. Moreover, which deenhancement the selectivity of the relay during high fault resistance. In [14], the protection methodology based on apparent resistance has been proposed. Howsoever, the final decision to derive trip command relies on threshold value which may be system dependent. [15, 16] introduced the travelling

wave-based protection method for multi-terminal DC microgrids. Still, this method is immune to noise signal and not applicable for low voltage DC systems due to the shorter length of the line. The protection method implements the fault detection and location by using the difference in current samples and correlation coefficient, respectively [17]. The slope of fault current based protection technique for constant impedance load microgrids has been proposed. However, it may not be the precise approach for high resistance faults [18]. [19] has addressed apparent resistance based protection techniques. However, this method is restricted to low resistance shunt faults and expects an additional auxiliary relay in case of high resistance faults, which leads to an increase in cost. Recently, the neural network based protection method to detect faults has been suggested [20, 21]. The parameter based protection method to locate the appropriate faulty section for smart microgrids has been explained [22]. [23], have presented a protection strategy by employing resistance to track the faults in the zonal DC microgrid. Despite that, this method may not be precise due to ignorance of effect of line inductance during fault study. In [24], the presented protection method adopts the concept of threshold resistance violation. However, the relay settings depend on the fault current direction, and it may fail for low magnitude fault currents.

In this paper, the unit protection scheme for ring configured DC microgrid has been presented. The proposed method continuously acquires the voltage and current samples and estimates the change in inductance (CI) by employing (9). The estimated CI at each protection device in the system holds zero value during normal operating conditions and conversely, CI has a non-zero value at the immediate inception of fault and sudden change in load conditions. Subsequently, with the help of sign of CI, the appropriate classification of internal, external faults and change in load has been accomplished. The proposed method has been tested for various abnormal conditions like the impact of fault resistance and location of the fault, effect of disconnection of line, source outage and the effect of sudden load change.

2 Proposed Protection Technique

The schematic diagram of the six terminal ring configuration DC microgrid is under test, as given in Figure 1. The system ratings of the tested microgrid are listed in Table 1. The DC microgrid constitutes solar PV, battery for storage, wind turbine, alternate current (AC) load, DC load, and AC grid. All resources and loads are interfaced to the DC grid through appropriate

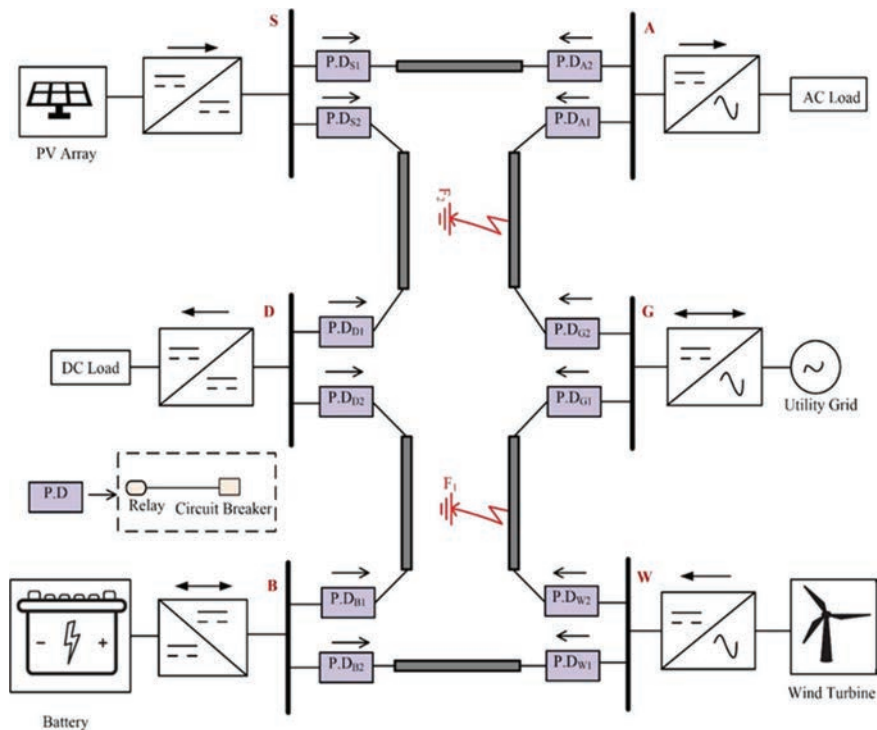


Figure 1 Architecture of six-terminal DC microgrid.

Table 1 Test system data [27]

Parameter	Ratings
System voltage	350 V
Base Power	500 kW
Battery	96V, 0.4kAh
Battery converter	125 kW
Solar panel	$V_{mp} = 54.7V, I_{mp} = 5.58A, P_{max} = 305 W$
PV DC-DC converter	125 kW
Wind turbine	500 kW
VSC interfaced to grid	250 kW
Resistance	0.125 Ω /km
Inductance	0.97 mH/km
Capacitance	12.1 mF/km
Constant Impedance Load	250 kW
Single-phase AC load	250 kW, 0.8 power factor lagging

converters, where solar PV and wind turbine generates maximum power with the help of maximum power point tracking (MPPT) technique [25]. The battery works as a backup source for power management and controlled using a bidirectional DC-DC converter [26]. Each line segment of the network is modelled as II-network. Each line terminal is associated with a voltage sensor, current sensor, and protection device (PD) to provide an appropriate trip signal to the breakers.

2.1 Fault Line Identification and Isolation

Due to the shorter length of line, low value of line resistance, and interfaced power electronic converters, the protection algorithm needs to produce a trip signal faster. This paper proposes the flow of the proposed method, as illustrated in Figure 2. To begin with, by using the local values of voltage and current, the inductance has been estimated. The non-zero inductance value corroborates that system subjected to the disturbance. Further, it is necessary to discriminate internal and external faults to enhance the selectivity of the protection system. If both the end protection devices (PDs) in a line detect a fault in the forward direction, it is confirmed as internal fault by PDs. However, for external fault, one end of the protection device (PD) senses the fault in the forward direction and the other end PD observes the same fault in the reverse direction [5, 27]. In this connection, the fault analysis has been performed by considering faults F_1 and F_2 in the lines GW and GA, respectively, as shown in Figure 1. For a detailed understanding, the three bus system is considered (part of tested microgrid) as depicted in Figures 3 and 4. Assume that pre-fault current is directed from bus G to W.

2.1.1 Internal fault analysis

When the system is operating under normal or steady operating conditions, the voltage at PD_{G1} in the line GW is

$$V_G = I_{G1}R_{GW} + V_W \quad (1)$$

V_G and V_W are pre-fault voltages measured at the PD_{G1} and PD_{W2} , respectively, R_{GW} is the total resistance of the GW line, and I_{G1} is current measured at PD_{G1} .

For the pole-ground fault (F_1), as shown in Figure 3, the voltage at PD_{G1} during transient conditions is

$$V_G^{F_1} = I_{G1}^{F_1}R_{GF} + L_{GF} \frac{d(I_{G1}^{F_1})}{dt} + V^{F_1} \quad (2)$$

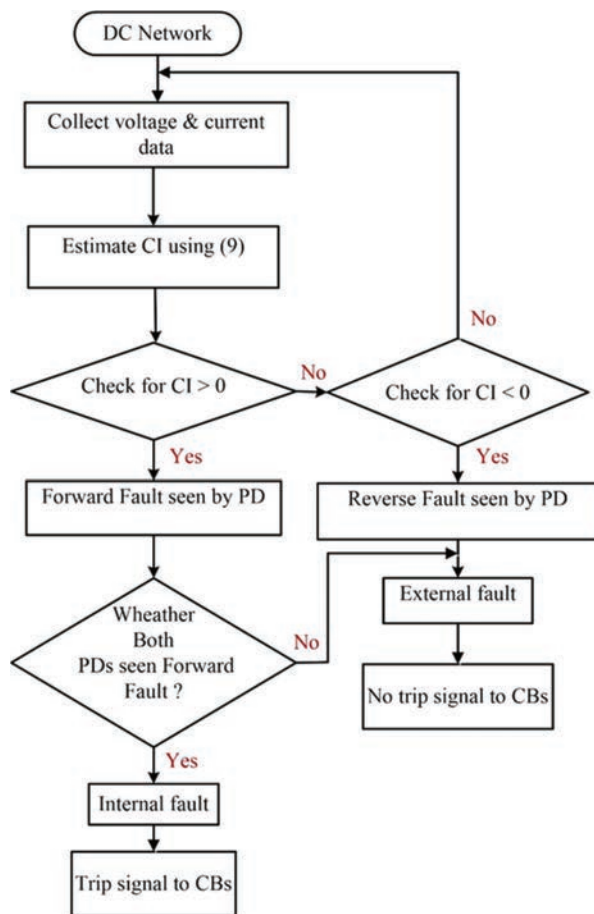


Figure 2 The flowchart of proposed protection method.

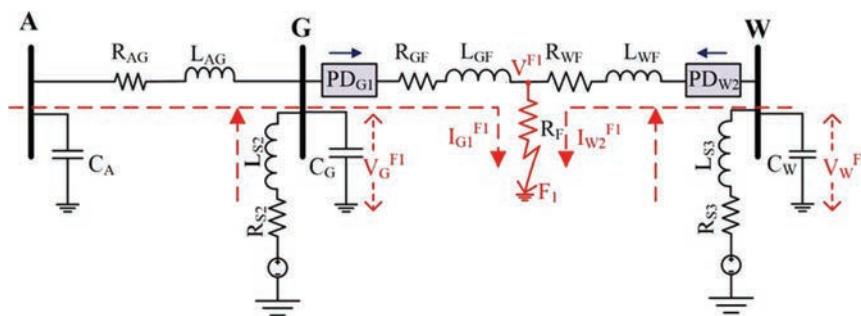


Figure 3 Model for internal fault analysis.

where, $V_G^{F_1}$ and V^{F_1} are voltages sensed at PD_{G1} and fault point, respectively. R_{GF} and L_{GF} are resistance and inductance from PD_{G1} to fault location (F_1).

Using (1) and (2)

$$\Delta V_G^{F_1} = I_{G1}^{F_1} R_{GF} + V^{F_1} - V_W + L_{GF} \frac{d(I_{G1}^{F_1})}{dt} - I_{G1} R_{GW} \quad (3)$$

where, $\Delta V_G^{F_1} = V_G^{F_1} - V_G$, it represents the change in voltage observed by PD_{G1} during the fault and (3) can be written in matrix as

$$\begin{bmatrix} I_{G1}^{F_1} & 1 & \frac{d(I_{G1}^{F_1})}{dt} & -I_{G1} \end{bmatrix} \begin{bmatrix} R_{GF} \\ V^{F_1} - V_W \\ L_{GF} \\ R_{GW} \end{bmatrix} = [V_G^{F_1} - V_G] \quad (4)$$

Similarly, expression at PD_{w2} during F_1 is

$$\begin{bmatrix} I_{W2}^{F_1} & 1 & \frac{d(I_{W2}^{F_1})}{dt} & -I_{W2} \end{bmatrix} \begin{bmatrix} R_{WF} \\ V^{F_1} - V_G \\ L_{WF} \\ R_{GW} \end{bmatrix} = [V_W^{F_1} - V_W] \quad (5)$$

where, I_{W2} and $I_{W2}^{F_1}$ are the pre-fault and fault currents noted at PD_{W2} , respectively, V_W and $V_W^{F_1}$ are the pre-fault and fault voltages at bus W , respectively, R_{WF} and L_{WF} are resistance and inductance from PD_{W2} to fault location (F_1).

2.1.2 External fault analysis

For the ground fault (F_2) in the line GA as depicted in Figure 4, the voltage at PD_{G1} is

$$V_G^{F_2} = -I_{G1}^{F_2} R_{GW} - L_{GW} \frac{d(I_{G1}^{F_2})}{dt} + V_W^{F_2} \quad (6)$$

where, $I_{G1}^{F_2}$ is current measured at PD_{G1} during F_2 , $V_G^{F_2}$ and $V_W^{F_2}$ are the voltages measured at PD_{G1} and PD_{w2} , respectively. L_{GW} and R_{GW} represents the inductance and resistance of the GW line.

Using (1) and (6), the change in voltage observed at PD_{G1} is

$$\Delta V_G^{F_2} = -I_{G1}^{F_2} R_{GW} + V_W^{F_2} - V_W - L_{GW} \frac{d(I_{G1}^{F_2})}{dt} - I_{G1} R_{GW} \quad (7)$$

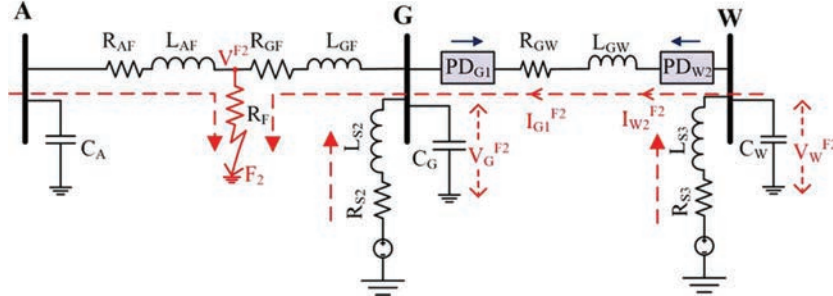


Figure 4 Model for external fault analysis.

Similarly, the change in voltage observed at PD_{W2} is

$$\Delta V_W^{F_2} = I_{W2}^{F_2} R_{GW} + V_G^{F_2} - V_G + L_{GW} \frac{d(I_{W2}^{F_2})}{dt} + I_{W2} R_{GW} \quad (8)$$

Using the Least Square Estimation method, the expressions (4), (5), (7), and (8) would be solved. It reveals that in the case of a forward fault (F_1), both PD_{G1} and PD_{W2} carry positive inductance coefficients. But for a reverse fault (F_2), PD_{G1} and PD_{W2} have a negative and positive coefficient, respectively. The estimation of change in inductance (CI) as follows

$$CI = \frac{\Delta L}{\Delta t} = \sum_{k=1}^8 \frac{L_{k+1} - L_k}{t_{k+1} - t_k} \quad (9)$$

Eight consecutive samples of inductance at a sampling rate of 8000 Hz have been considered to estimate change in inductance. From this information, the sign of CI is positive and negative for forward fault and reverse fault, respectively. Moreover, if both end protection devices hold positive signs, the fault is treated as an internal fault and allows the corresponding circuit breakers to operate; otherwise, the fault is external and no operating signal is issued to the breakers.

2.2 Protection Arrangement for Isolation of Faulty Line

The protection arrangement between two protection devices located on both terminals of the line plays an essential role in enhancing the selectivity and reliability of the protection system. The effective protection arrangement for the trip signal generator is illustrated in Figure 5. Appropriate isolation of faulty line enhances the continuity in power supply to the consumers to

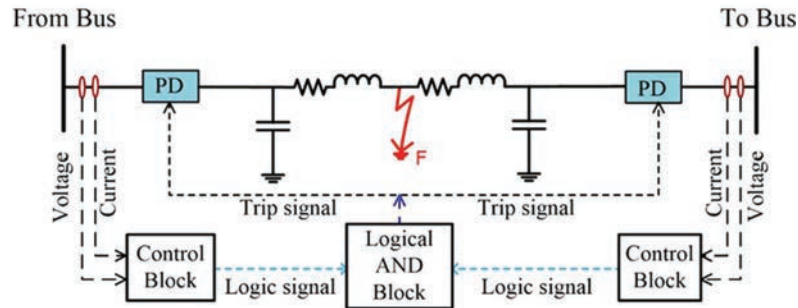


Figure 5 Protection arrangement for isolation of faulty line.

increase the reliability of the microgrid. By employing local current and voltage samples data, the polarity of change in inductance is computed using (9) immediately after fault initiation. The polarity of computed change in inductance is positive for forward fault and the control block produces logic signal '1'. The other way around, computed inductance holds a negative value for reverse fault and logic signal '0' has been produced.

In case of the internal fault, the logic signal produced by both control blocks would be logic '1', and as a result, the logical AND block will issue trip signals to breakers to isolate the faulty line. For external fault, anyone of the control blocks obtains logic '0' and results in no function of circuit breakers.

3 Results and Discussions

The technique is proposed for the detection and isolation of fault for multi-terminal DC microgrid has been modelled and simulated using Matlab/Simulink tool and the response of the grid model under different fault conditions is analysed. The genuineness of the proposed protection method has been simulated and verified on a six terminal DC microgrid during dissimilar abnormal conditions.

3.1 Internal Fault Case

A pole-ground fault with fault resistance of 0.1Ω is placed in the GW line at a distance of 0.2 km from bus G at the time $(t) = 0.4$ s, as shown in Figure 1. The three bus system has been considered for this fault study, as depicted in Figure 3. The current and voltage waveforms at PD_{G1} and PD_{W2} are shown in Figure 6.

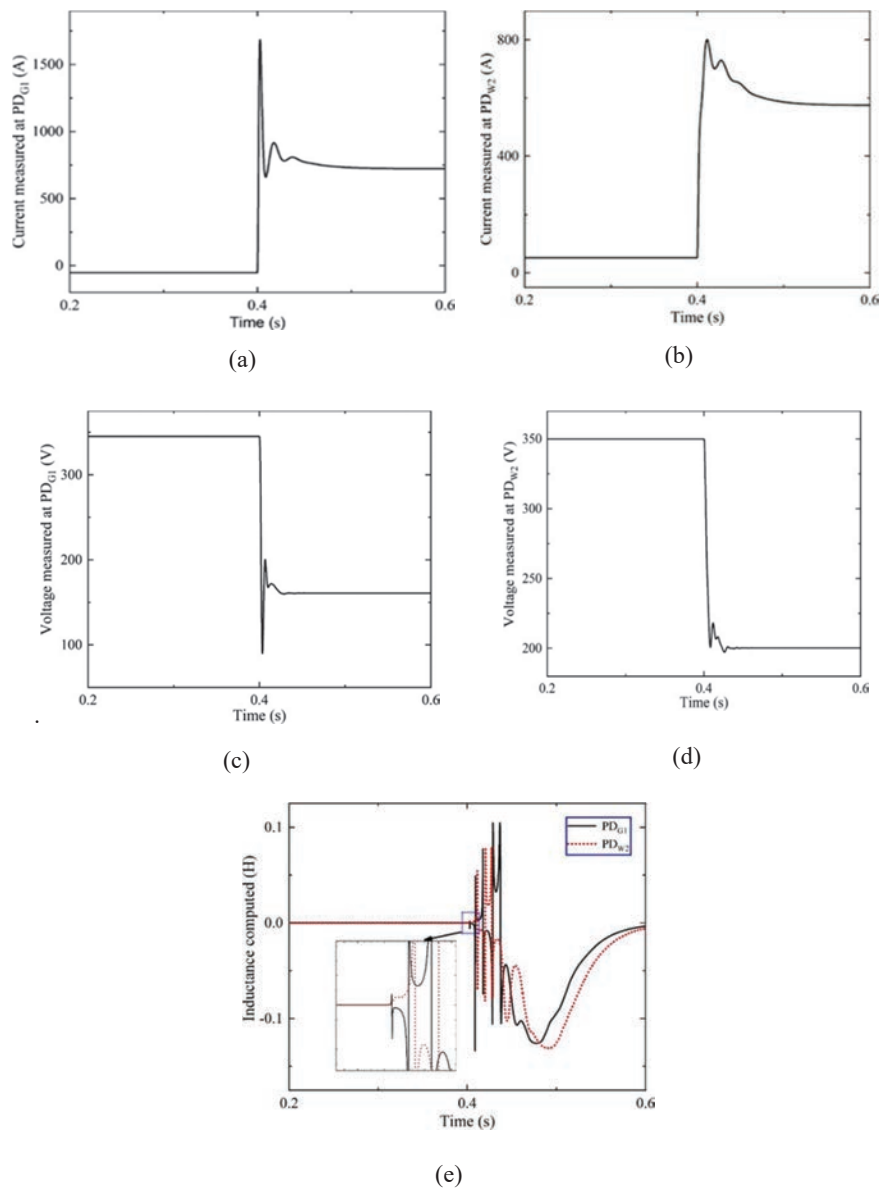


Figure 6 Current measured at (a) PD_{G1} (b) PD_{W2}, Voltage measured at (c) PD_{G1} (d) PD_{W2}, (e) Inductance computed at PD_{G1} and PD_{W2}.

From the results, the voltage, current values are committed with transients, and an increment in the current, decrement in voltage has been observed. As the fault is located nearer to PD_{G1} , the impact of fault at PD_{G1} is more as compared to PD_{W2} . During the disturbance, both end protection devices compute inductance, as shown in Figure 6(e).

Subsequently, the change in inductance is calculated by employing (9) and it is seen that both PD_{G1} and PD_{W2} hold positive values immediately after initiation of fault. The concern relays identified the fault in the forward direction and corroborated that the fault is internal. Consequently, the two relays associated with the fault line feed the enable signal to logic AND block, which grant trip signals to concern breakers. Hence, this protection approach effectively isolates the faulty line from the microgrid.

3.2 External Fault Case

The ground fault with $R_F = 1 \Omega$ is created at 0.5 km distance from bus A in AG line at time $(t) = 0.4$ s as shown in Figure 5. During this fault case, concern PDs sense changes in the voltage and current have presented in Figure 7. This fault study reveals that, a uniform change in current at both PD_{G1} and PD_{W2} and these currents contains transient rise and dip. As the fault is located closer to PD_{G1} , Consequently, the reduction in voltage at PD_{G1} is slightly more than the voltage at PD_{W2} .

Figure 7(e) shows the computed values of inductance at PD_{G1} and PD_{W2} and the change in inductance is calculated by adopting (9). It demonstrates that the computed value at PD_{G1} and PD_{W2} carries negative and positive values, respectively, immediately after fault initiation. It confirms as the PD_{G1} is sensed the fault in the AG line as a reverse fault and the same fault treated as forward fault concerned to the PD_{W2} . The concern relays identified the fault in the forward direction and corroborated that the fault is internal. Consequently, the PD_{G1} and PD_{W2} produce logic '1' and '0', respectively. The logic AND block will not grant trip signals to concern breakers. Hence, this proposed protection approach improves the selectivity of the protection system.

3.3 Impact of Fault Resistance

The proposed protection algorithm has been examined by considering the pole-ground fault in the WB line at 0.4 km distance from bus W and fault

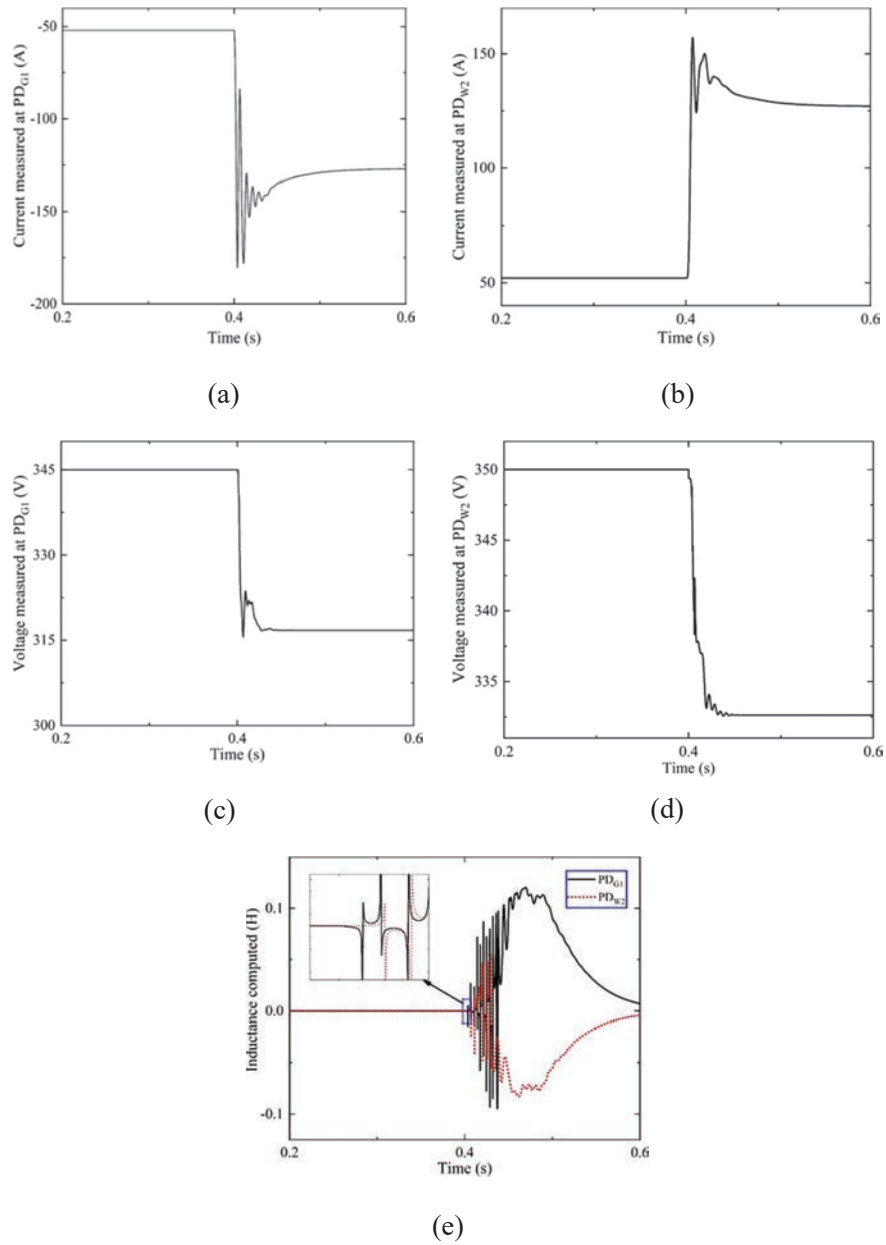


Figure 7 Current measured at (a) PD_{G1} (b) PD_{W2}, Voltage measured at (c) PD_{G1} (d) PD_{W2}, (e) Inductance computed at PD_{G1} and PD_{W2}.

resistance (R_F) value ranging from 0Ω to 15Ω . The voltage and current waveforms as shown in Figure 8.

From this fault investigation, when fault resistance increases, then the fault current decreases. Concurrently, the value of voltage measured at relay will increase with fault resistance. From Figure 8(e) & (f), the computed inductance at PD_{W1} and PD_{B2} have positive values immediately at fault inception for different fault resistance. Consequently, the corresponding protection devices confirm the fault as internal fault, and appropriate signal would be issued to operate breakers.

3.4 Impact of Fault Location

A fault in the WB line with $R_F = 0.5 \Omega$ is simulated for various fault locations to examine the proposed algorithm. In this case, the location of the fault is represented by 'P' w.r.t. PD_{W1} . The currents and voltages sensed at PD_{W1} and PD_{B2} have presented in Figure 9. When the fault location moves towards another end of the same line segment, the values of current and voltage decrease and increase, respectively, and there is a reduction in current transients. It noted that the location of the fault also affects the system performance.

Figure 9(e) & (f) shows that for all the cases, the computed value of inductance by concern PDs remains positive, and the proper operation of breakers takes place to isolate the line. Hence, the accuracy of the proposed method is not affected by the fault location, which will improve the dependability of relay.

3.5 Radial Configuration

This protection method is also simulated for the sudden removal of the line segment due to its maintenance. The DS line is disconnected at $t = 0.4$ s from rest of the system to test the functionality of the proposed method during unhealthy conditions. The current measured values at PD_{D1} and PD_{S2} are presented in Figure 10.

The computed inductance at various protection devices is displayed in Figure 10(b) and by using (9) the sign of CL has been obtained. Figure 10(b) it confirms that PD_{W1} , PD_{B1} , PD_{A2} , PD_{G2} have positive inductance values and heeded the disturbance in the forward direction.

However, PD_{B2} , PD_{D2} , PD_{S1} , PD_{A1} , PD_{G1} , PD_{W2} have negative inductance values and detect the disturbance in the reverse direction.

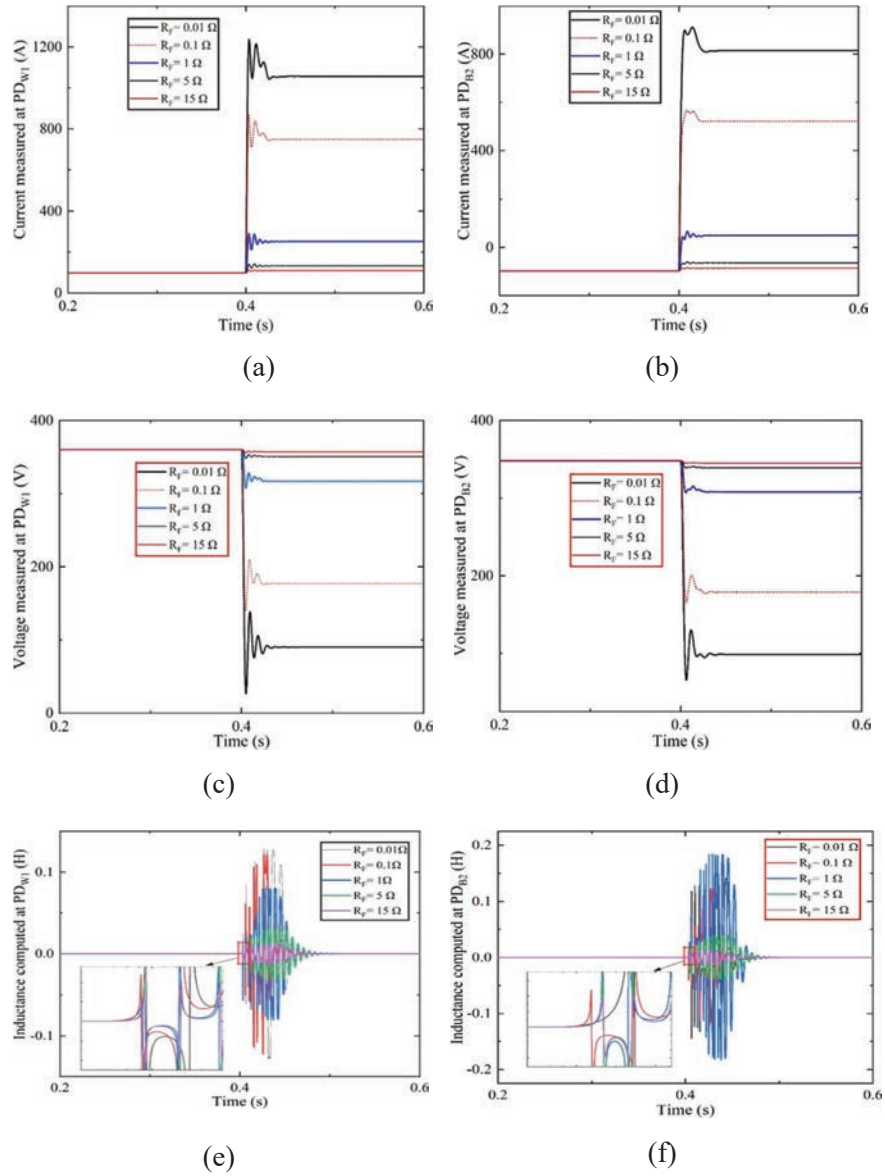


Figure 8 Current measured at (a) PD_{W1} (b) PD_{B2}, Voltage measured at (c) PD_{W1} (d) PD_{B2}, Inductance computed at (e) PD_{W1} (f) PD_{B2}.

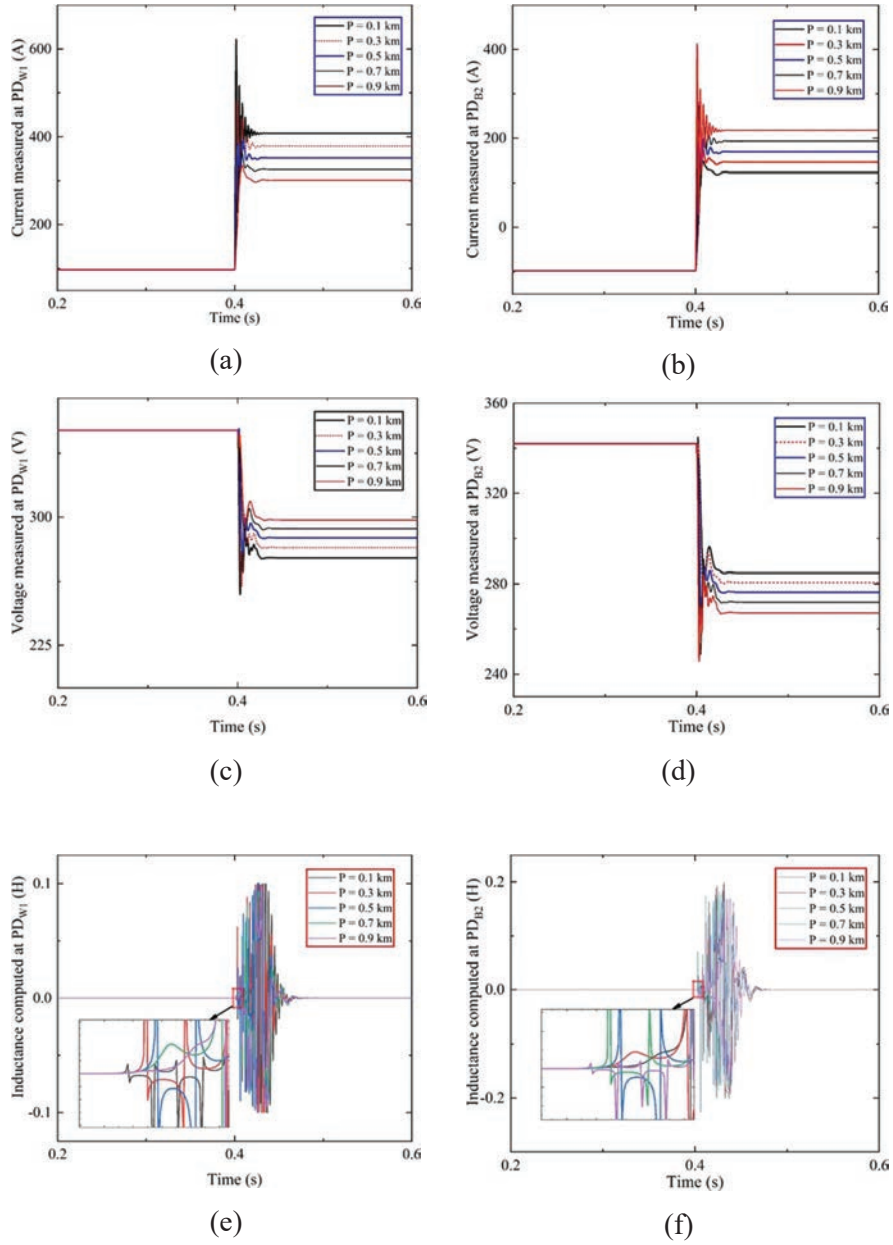


Figure 9 Current measured at (a) PD_{W1} (b) PD_{B2}, Voltage measured at (c) PD_{W1} (d) PD_{B2}, Inductance computed at (e) PD_{W1} (f) PD_{B2}.

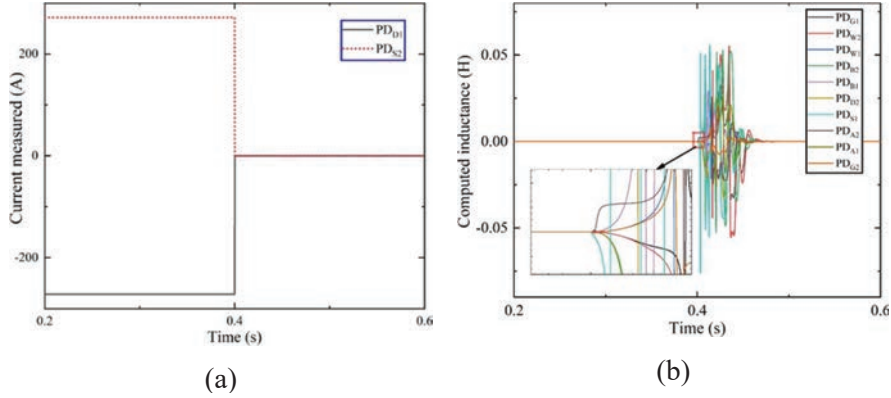


Figure 10 (a) Current measured at PD_{D1} and PD_{S2} (b) Inductance computed at all PDs.

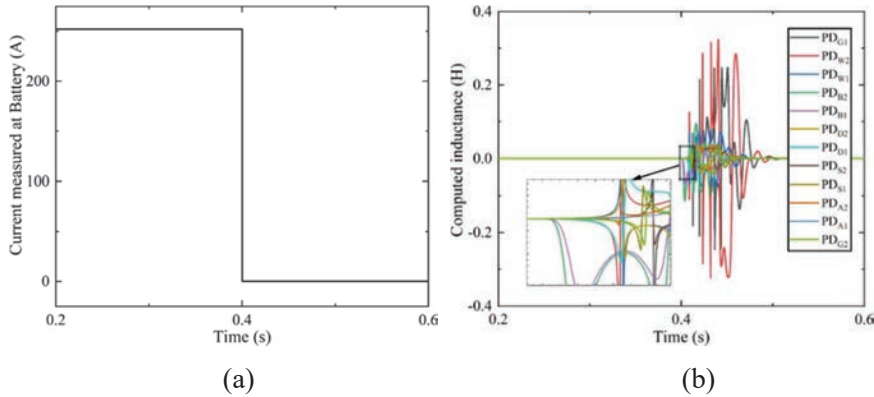


Figure 11 (a) Current measured at battery terminal (b) Inductance computed at various PDs.

3.6 Effect of Source Outage

Consider the battery is out of service due to service maintenance and during such case, the current supplied by the battery source becomes zero at $t = 0.4$ s, as shown in Figure 11. The inductance computed at all PDs is displayed during this validation process in Figure 11. Immediately after the disturbance, PD_{W1}, PD_{G1}, PD_{A2}, PD_{S2}, PD_{D2} hold positive inductance values and identified the disturbance as a forward fault. However, PD_{B2}, PD_{W2}, PD_{G2}, PD_{A1}, PD_{S1}, PD_{D1}, PD_{B1} owned the negative values of inductance and disturbance identified as a reverse fault.

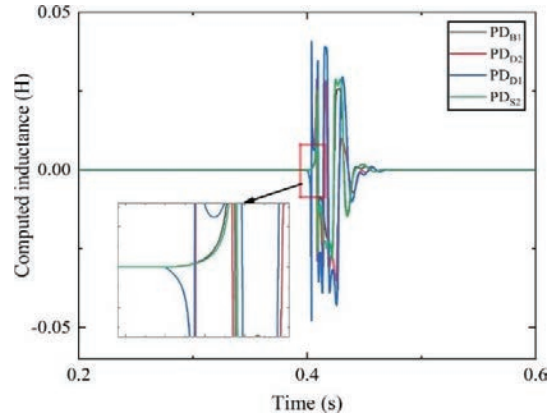


Figure 12 Inductance computed during sudden load change.

3.7 Sudden Change in Load

To examine the protection algorithm to enhance security, the disturbance in load is created at $t = 0.4$ s at bus D. The simulation has been carried out for overloading conditions like 150% of its rated load.

Under these conditions, the computed inductance values at PD_{B1} and PD_{S2} carry a positive identity. Simultaneously, PD_{D2} and PD_{D1} have a negative identity, as shown in Figure 12. Hence the proposed algorithm will not respond to the sudden change in the load, strengthening the security of the protection system.

4 Conclusion

The protection of ring configuration DC microgrid plays a crucial role in the distributed system because of the current limiting nature of converters and bi-directional power flow. This research proposes an accurate and reliable protection scheme for a ring configured DC microgrid that includes detection of disturbances like fault and sudden load changes. This method also identifies and isolates the faulty line for reliable operation. In the proposed method, the sign of CI is used to categorize internal and external faults with accurate communication between PDs on both ends. The proposed protection scheme has been tested on a 6-Bus ring configured DC microgrid in MATLAB/Simulink tool for several dissimilar abnormal conditions such as low and high resistance magnitude faults, the impact of fault location in

a line segment, sudden removal of the line, inactive operation of solar PV due to natural variation in solar irradiation and sudden switching operation of loads. From the fault study, it is noted that the proposed protection algorithm has improved the selectivity, dependability, security and reliability. This method is found to be fast and accurate during the aforementioned cases as a consequence the detriment of power electronic switches can be prevented.

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