Improved Performance of Dual Active Bridge Converter using Particle Swarm Optimization based Phase Shift Modulation for EV Application

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Abstract

The five-level dual active bridge (FLDAB) topology is recently presented to suppress the harmonic content in the high frequency link (HFL) of DC-DC converter. However, the conventional FLDAB topology requires additional four diodes and one switch for the generation of five-level at the output. These four diodes and one switch cause losses in the system and hence the efficiency of the system decreases. Keeping the drawbacks of conventional FLDAB topology in view, this paper presents a novel FLDAB topology with the lower component count i.e., two switches only. The proposed FLDAB topology based DC-DC converter implements PSO based modulation for electric vehicle application. This paper presents a detailed analysis of the proposed FLDAB topology. Further, the analysis involves a comparative

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evaluation against conventional FLDAB topology. The comparative results shows that the proposed topology produces lesser harmonics in the HFL of the DC-DC converter and it is more efficient than the conventional FLDAB topology. Thus presenting a promising and improved solution for DC-DC converters in electric vehicle application. The OPAL-RT hardware-in-loop emulator validates the obtained results.

Keywords: Multilevel dual active bridge (MLDAB), high frequency link (HFL), total harmonic distortion (THD), particle swarm optimization (PSO) algorithm.

1 Introduction

The need for awareness of environmental issues and strict rules to reduce greenhouse gas emissions have accelerated the push for environmental friendly modes of transportation. Consequently, the automotive industry is experiencing a notable shift from conventional internal combustion engine based vehicle technology to electrification. The growing adoption of electric vehicles (EVs) and advancements in charging infrastructure drive this transition [1]. However, the lack of sufficient charging infrastructure and the lack to meet the international charging standards not only restrain the expansion of EVs but also increase the quantity of charging infrastructure with subpar performance [2, 3]. The majority of existing charging methods do not meet the international requirements. Low power factor and high total harmonic distortion (THD) are all indicators of poor performance [4]. Increasing the need for a universal charging system for all EVs, implementation of a number of different single stage and two stage charger topologies for EVs has been the subject of research [5, 6]. As in current chargers the performance metrics of interest include the input power factor, distortion factor, displacement factor and charger efficiency, all degrade when diode bridge rectifier is used in conjunction with a dc-link capacitor. Generally, better performance characteristics have been demonstrated for two-stage designs. To enhance the power quality of an AC-DC conversion system, active power factor correction (APFC) circuits based on boost converters have gained widespread adoption in medium to high power applications [7, 8]. However, their usefulness was constrained by a few factors, prompting researchers to look for alternatives. Therefore, a number of APFC implementations using a variety of converters deriving from the buck-boost topology as in references [9, 10]. However, their application is constrained at low to medium power levels because of

the high current stress, huge filter demand and more number of devices being used. The use of interleaved cells appears favourable at high power application as mentioned in [11, 12]. Nevertheless, the increase in the large filter requirement and increase in device count persists.

It is crucial to have power converters for EV applications that have galvanic isolation and the bidirectional flow of power. Multiple configurations of isolated bidirectional DC-DC converters (IBDCs) are possible [13–15]. Due to its inherent ability of soft switching without using any auxiliary components, the DAB converter is the best IBDC for power applications like battery management systems, EVs, solid-state transformers and DC distribution system interface. Many indices frequently impact the performance of the DAB converter, including increased current stress on the HFL device due to harmonics in the inductor current. The harmonics also cause the HFT and the devices to overheat, hence decrease in efficiency of the converter. The achievement of high efficiency and reliability in DAB can be attained by making modifications to the performance indices via the modulation schemes and circuit architecture [16]. Single phase shift (SPS) modulation is widely recognized as the most prevalent modulation technique. However in SPS modulation technique, the converter experiences significant current stress and limited soft-switching range [17]. In order to address these challenges, researchers have developed different modulation techniques including extended phase shift (EPS) modulation [18], dual-phase shift (DPS) modulation [19], and triple-phase shift (TPS) modulation [20]. In addition to the aforementioned modulation systems, there are alternative methods such as hybrid modulation as discussed in [21]. However, these techniques produce much harmonics in the HFL of the DAB converter. Therefore, the efficiency of the converter reduces.

In order to reduce the THD of the HFL current waveform, multilevel topologies are used by different researchers at the either end of the DAB converter. In [22], the authors provide a solution to operate multilevel DAB converter consists of neutral point clamped configuration having different levels. Further, in order to reduce the inductor current THD and to achieve this, an additional four active switches are employed to generate a five-level voltage waveform which reduces the efficiency of the system [23]. A modulation technique with additional degrees of freedom used to minimize harmonics. However, this improvement required the addition of four extra components on both sides of the converter [24]. Further, in [25] a transistor clamped FLDAB converter is proposed with voltages of two and five level due to three degrees of freedom which improves its ability to regulate power

flow, and the inductor current THD reduces. Also the performance evaluation of converter topology, incorporating five voltage levels on both sides of the HFT, therefore diminishing the inductor current harmonics [26]. Further, the QPS-modulation based topology, incorporating auxiliary switch. This design aids in mitigating the inductor current harmonics [27]. However for generating five-level in [25–27], additional components (switches & diodes) are required, therefore compromising their efficiency. Keeping the above mentioned drawback in view, the authors have presented a novel FLDAB topology using PSO based modulation technique for EV application. This study outlines the following primary contributions:

- A novel FLDAB converter topology using PSO algorithm based modulation technique has been developed.
- The performance of the proposed FLDAB converter using PSO based modulation technique and conventional FLDAB converter with QPS scheme has been compared.
- The comparative results shows that the proposed PSO modulation based converter produces lesser harmonics in the HFL of the DC-DC converter and it is more efficient than the conventional FLDAB converter.
- The results achieved are validated by OPAL-RT emulator.

The following sections organize the remainder of this work as follows:

Sections 2 and 3 illustrates the conventional converter and its control strategy. Sections 4 and 5, deals with topology and the control strategy of the proposed FLDAB converter using PSO based modulation. Section 6, deals with the simulation as well as real time results. Section 7, deals with the comparison illustration. Finally, a conclusion is drawn in Section 8.

2 Conventional Topology

HFT connects both the HV and LV side bridges. The four active switches (S_1–S_4) integrated with antiparallel diode (D_1–D_4), a bidirectional auxiliary switch (X) along with four diodes $D_{11} - D_{44}$), complete the LV side-bridge. The four active switches ($S_5 - S_8$) with incorporated antiparallel diodes ($D_5 - D_8$) complete the HV side bridge. v_{hv} and v_{lv} denote the AC voltages of the bridges. The turns ratio of the HFT is represented by "$1 : n$" and the capacitances are C_1, C_2, and C_3. "v_L" and "i_L" denote the inductor voltage and current respectively as illustrated in Figure 1.

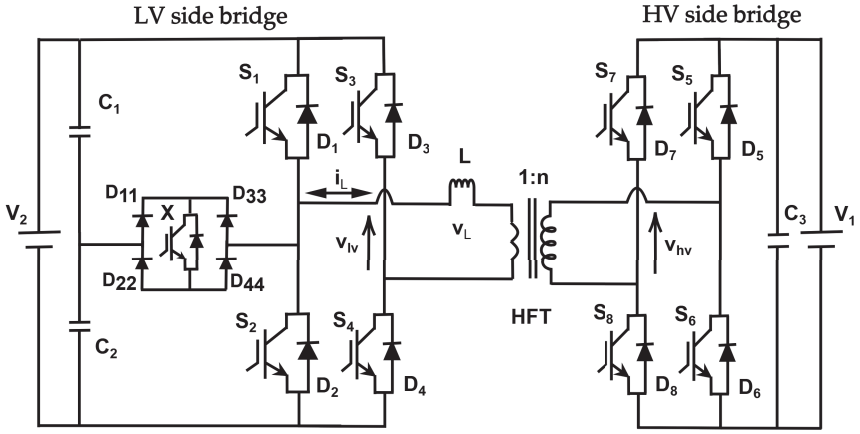

Figure 1 Schematic of the conventional converter.

3 Control Strategy of Conventional Converter

Figures 2 and 3, depict the operation of the conventional MLDAB converter. To have desired voltage levels in both the modes of operation it is essential to adjust the switching status in the HV and LV side bridge configurations as below, The G2V operation at different instants is illustrated in Figure 2(a–g). The turn-on of switches S_5 and S_8 in HV side bridge. In the LV side bridge, S_1 and S_3 switches turn on during the time interval from t_0 to t_1 as depicted in Figure 2(a). The turn-on of switches S_5 and S_8 in HV side bridge. In the LV side bridge, X and S_4 switches turn on during the time interval from t_1 to t_2 as depicted in Figure 2(b). The turn-on of switches S_5 and S_8 in HV side bridge. In the LV side bridge, S_1 and S_4 switches turn on during the time interval as shown in Figure 2(c). The turn-on of switches S_5 and S_7 in HV side bridge. In the LV side bridge, S_1 and S_4 switches turn on during the time interval from t_3 to t_4 as depicted in Figure 2(d). The turn-on of switches S_5 and S_7 in HV side bridge. In the LV side bridge, X and S_4 switches turn on during the time interval from t_4 to t_5 as depicted in Figure 2(e). The turn-on of switches S_6 and S_7 in HV side bridge. In the LV side bridge, X and S_4 switches turn on during the time interval from t_5 to t_6 as depicted in Figure 2(f). The turn-on of switches S_6 and S_7 in HV side bridge. In the LV side bridge, S_2 and S_4 switches turn on during the time interval from t_6 to t_7 as depicted in Figure 2(g). Furthermore, for the forward mode of operation the switching states as shown in Table 1, has been made according to the above mentioned operation.

Table 1 G2V states of switches of conventional converter

Switching States	Modes													
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
S_1	1	0	1	1	0	0	0	0	0	0	0	0	0	1
S_2	0	0	0	0	0	0	1	1	0	1	1	0	0	0
S_3	1	0	0	0	0	0	0	0	1	1	1	1	1	1
S_4	0	1	1	1	1	1	1	1	0	0	0	0	0	0
S_5	1	1	1	1	1	0	0	0	0	0	0	0	1	1
S_6	0	0	0	0	0	1	1	1	1	1	1	1	0	0
S_7	0	0	0	1	1	1	1	1	1	1	0	0	0	0
S_8	1	1	1	0	0	0	0	0	0	0	1	1	1	1
X	0	1	0	0	1	1	0	0	1	0	0	1	1	0

The V2G operation at different instants is illustrated in Figure 3(a–g). The turn-on of switches S_5 and S_8 in HV side bridge. In the LV side bridge, S_1 and S_3 switches turn on during the time interval from t_0 to t_1 as depicted in Figure 3(a). The turn-on of switches S_5 and S_8 in HV side bridge. In the LV side bridge, X and S_3 switches turn on during the time interval from t_1 to t_2 as depicted in Figure 3(b). The turn-on of switches S_6 and S_8 in HV side bridge. In the LV side bridge, X and S_3 switches turn on as shown in Figure 3(c). The turn-on of switches S_6 and S_8 in HV side bridge. In the LV side bridge, S_2 and S_3 switches turn on during the time interval from t_3 to t_4 as depicted in Figure 3(d). The turn-on of switches S_6 and S_7 in HV side bridge. In the LV side bridge, S_2 and S_3 switches turn on during the time interval from t_4 to t_5 as depicted in Figure 3(e). The turn-on of switches S_6 and S_7 in HV side bridge. In the LV side bridge, X and S_3 switches turn on during the time interval from t_5 to t_6 as depicted at the last of in Figure 3(f). The turn-on of switches S_6 and S_7 in HV side bridge. In the LV side bridge, S_2 and S_4 switches turn on during the time interval from t_6 to t_7 as depicted at the last. Also, the states of switches as shown in Table 2 is made accordingly.

4 Proposed FLDAB Converter

HFT connects both the HV and LV side bridges. The four active switches (S_1–S_4) integrated with antiparallel diodes (D_1–D_4), and a bidirectional auxiliary switches (X_1, X_2) connects one of the midpoints of the H-bridge leg to the capacitor leg, completing the LV side bridge. The auxiliary switch consists of the two active switch (X_1, X_2) connected in antiparallel to each other. Four active switches ($S_5 - S_8$) and integrated antiparallel diodes

Table 2 V2G states of switches of conventional converter

Switching States	Modes													
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
S_1	1	0	0	0	0	0	0	0	0	0	1	1	0	1
S_2	0	0	0	1	1	0	1	1	0	0	0	0	0	0
S_3	1	1	1	1	1	1	0	0	0	0	0	0	0	0
S_4	0	0	0	0	0	0	1	1	1	1	1	1	1	0
S_5	1	1	0	0	0	0	0	0	0	1	1	1	1	1
S_6	0	0	1	1	1	1	1	1	1	0	0	0	0	0
S_7	0	0	0	0	1	1	1	1	1	1	1	0	0	0
S_8	1	1	1	1	0	0	0	0	0	0	0	1	1	1
X	0	1	1	0	0	1	0	0	1	1	0	0	1	0

($D_5 - D_8$) form the HV side bridge. v_{hv} and v_{lv} denote the voltages of the bridges. The turns ratio of the HFT is represented by "$1 : n$" and the capacitances are C_1, C_2, and C_3. "v_L" and "i_L"denote the inductor voltage and current respectively as illustrated in Figure 4.

5 Proposed PSO Based Modulation Control Strategy of FLDAB Converter

5.1 Operating Principle of Proposed FLDAB Converter

Figures 5 and 6, depict the operation of the proposed FLDAB converter. To have desired voltage levels in both the modes of operation it is essential to adjust the switching status in the HV and LV side bridge configurations as below, The G2V operation at different instants is illustrated in Figure 7. The turn-on of switches S_5 and S_8 in HV side bridge. In the LV side bridge, S_1 and S_3 switches turn on during the time interval from t_0 to t_1 as depicted in Figure 7(a). HV Side and LV side voltages are V_1 and 0 respectively. Current i_L increases and is expressed as,

$$i_L(t) = i_L(t0) + (V_1/n)/L \times (t_1 - t_0). \tag{1}$$

The turn-on of switches S_5 and S_8 in HV side bridge. In the LV side bridge, X and S_4 switches turn on during the time interval from t_1 to t_2 as depicted in Figure 7(b). HV Side and LV side voltages are V_1 and $V_2/2$ respectively. Current i_L increases and is expressed as,

$$i_L(t) = i_L(t_1) + (V_1/n - V_2/2)/L \times (t_2 - t_1). \tag{2}$$

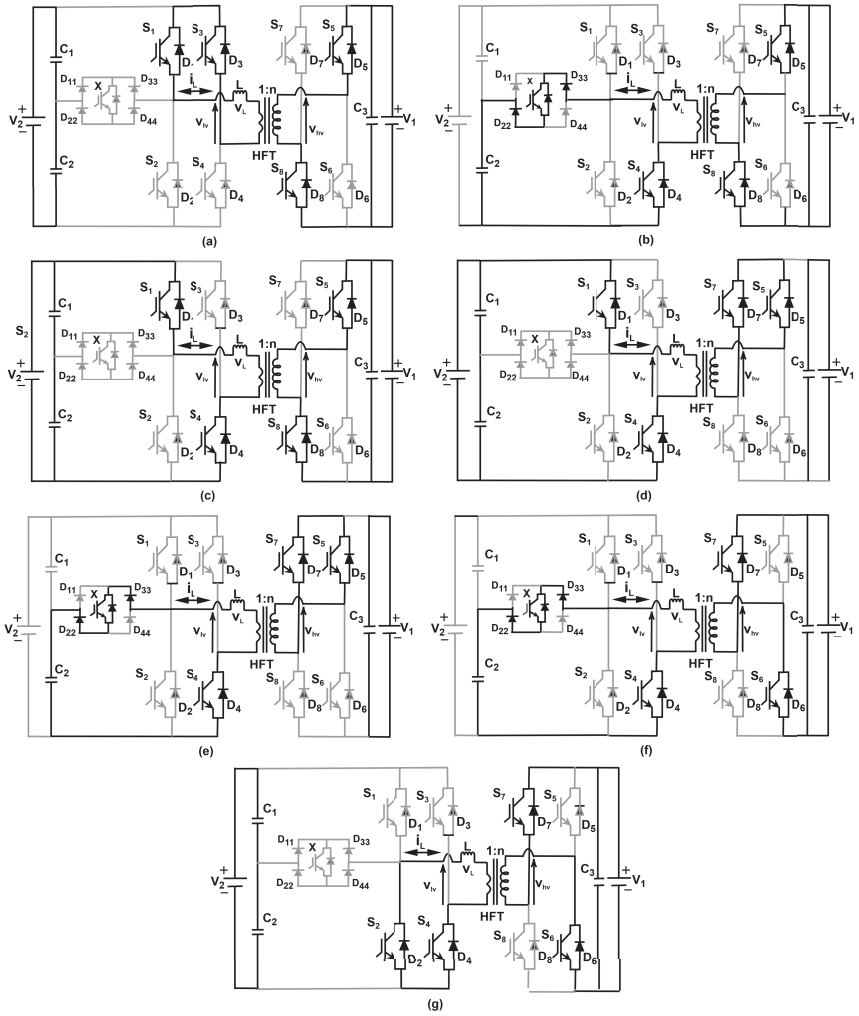

Figure 2 G2V operation of conventional converter.

The turn-on of switches S_5 and S_8 in HV side bridge. In the LV side bridge, S_1 and S_4 switches turn on as shown in Figure 7(c). HV Side and LV side voltages are V_1 and V_2 respectively. Current i_L increases and is expressed as,

$$i_L(t) = i_L(t_2) + (V_1/n - V_2)/L \times (t_3 - t_2). \tag{3}$$

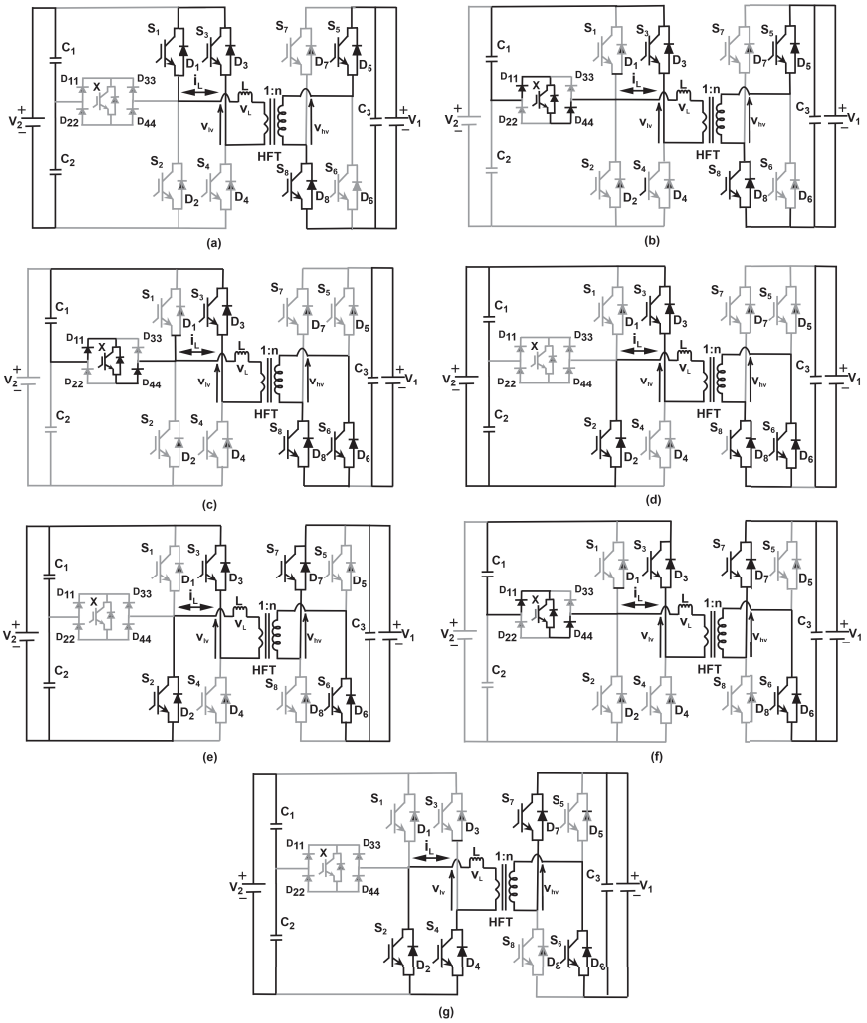

Figure 3 V2G operation of conventional converter.

The turn-on of switches S_5 and S_7 in HV side bridge. In the LV side bridge, S_1 and S_4 switches turn on during the time interval from t_3 to t_4 as depicted in Figure 7(d). HV Side and LV side voltages are 0 and V_2 respectively. Current i_L decreases and is expressed as,

$$i_L(t) = i_L(t_3) - (V_2)/L \times (t_4 - t_3). \tag{4}$$

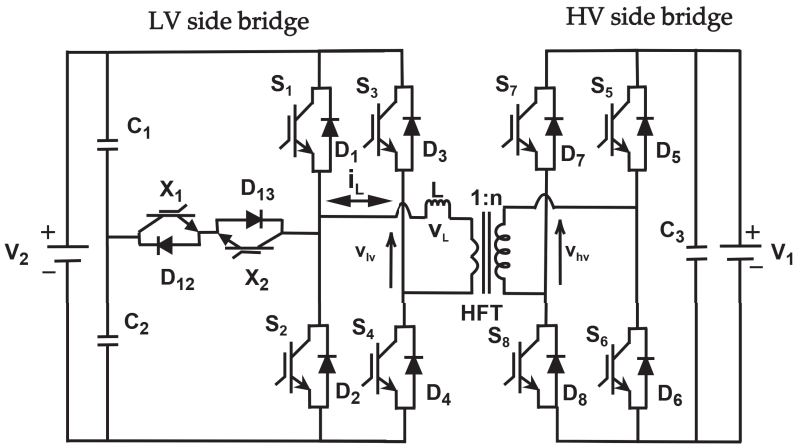

Figure 4 Schematic of proposed converter.

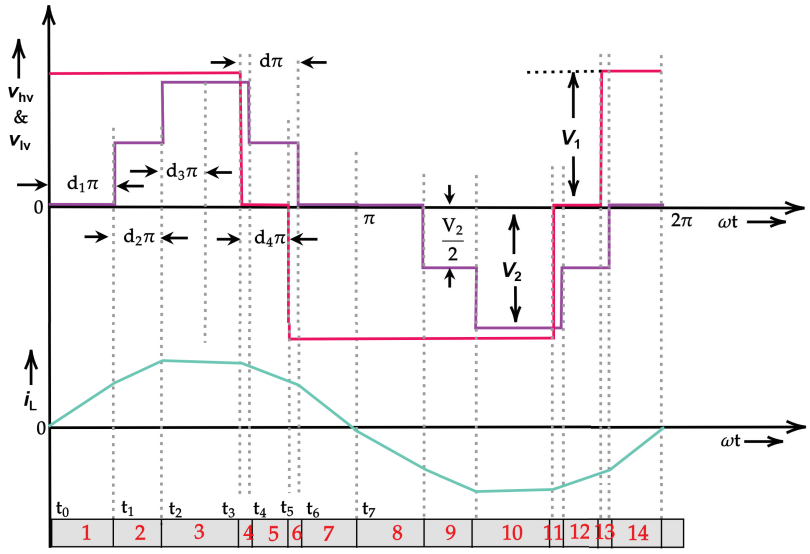

Figure 5 Proposed G2V operating waveforms.

The turn-on of switches S_5 and S_7 in HV side bridge. In the LV side bridge, X and S_4 switches turn on during the time interval from t_4 to t_5 as depicted in Figure 7(e). HV Side and LV side voltages are 0 and $V_2/2$ respectively. Current i_L decreases and is expressed as,

$$i_L(t) = i_L(t_4) - (V_2/2)/L \times (t_5 - t_4). \tag{5}$$

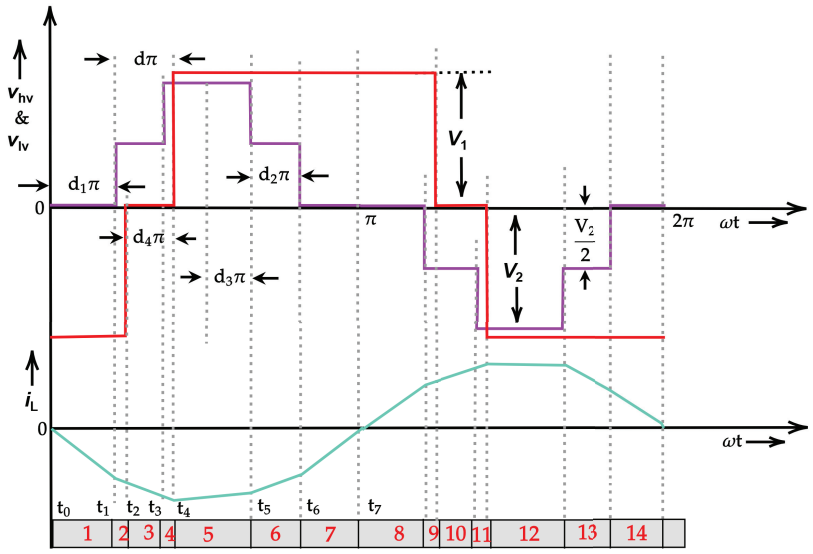

Figure 6 Proposed V2G operating waveforms.

The turn-on of switches S_6 and S_7 in HV side bridge. In the LV side bridge, X and S_4 switches turn on during the time interval from t_5 to t_6 as depicted in Figure 7(f). HV Side and LV side voltages are $-V_1$ and $V_2/2$ respectively. Current i_L decreases and is expressed as,

$$i_L(t) = i_L(t_5) - (V_1/n + V_2/2)/L \times (t_6 - t_5). \tag{6}$$

The turn-on of switches S_6 and S_7 in HV side bridge. In the LV side bridge, S_2 and S_4 switches turn on during the time interval from t_6 to t_7 as depicted in Figure 7(g). HV Side and LV side voltages are $-V_1$ and 0 respectively. Current i_L decreases and is expressed as,

$$i_L(t) = i_L(t_6) - (V_1)/L \times (t_7 - t_6). \tag{7}$$

Furthermore, for the forward mode of operation the switching states as shown in Table 3, has been made according to the above mentioned operation. The V2G operation at different instants is illustrated in Figure 8(a–g). The turn-on of switches S_5 and S_8 in HV side bridge. In the LV side bridge, S_1 and S_3 switches turn on during the time interval from t_0 to t_1 as depicted in Figure 8(a). HV Side and LV side voltages are $-V_1$ and 0 respectively. Current i_L increases in reverse direction and is expressed as,

$$i_L(t) = i_L(t_0) + (V_1)/nL \times (t_1 - t_0). \tag{8}$$

The turn-on of switches S_5 and S_8 in HV side bridge. In the LV side bridge, X and S_3 switches turn on during the time interval from t_1 to t_2 as depicted in Figure 8(b). HV Side and LV side voltages are $-V_1$ and $V_2/2$ respectively. Current i_L increases in reverse direction and is expressed as,

$$i_L(t) = i_L(t_1) + (V_2/2 + V_1/n)/L \times (t_2 - t_1). \tag{9}$$

The turn-on of switches S_6 and S_8 in HV side bridge. In the LV side bridge, X and S_3 switches turn on as shown in Figure 8(c). HV Side and LV side voltages are 0 and $V_2/2$ respectively. Current i_L increases in reverse direction and is expressed as,

$$i_L(t) = i_L(t_2) + (V_2/2)/L \times (t_3 - t_2). \tag{10}$$

The turn-on of switches S_6 and S_8 in HV side bridge. In the LV side bridge, S_2 and S_3 switches turn on during the time interval from t_3 to t_4 as depicted in Figure 8(d). HV Side and LV side voltages are 0 and V_2 respectively. Current i_L increases in reverse direction and is expressed as,

$$i_L(t) = i_L(t_3) + (V_2)/L \times (t_4 - t_3). \tag{11}$$

The turn-on of switches S_6 and S_7 in HV side bridge. In the LV side bridge, S_2 and S_3 switches turn on during the time interval from t_4 to t_5 as depicted in Figure 8(e). HV Side and LV side voltages are V_1 and V_2 respectively. Current i_L decreases and is expressed as,

$$i_L(t) = i_L(t_4) + (V_2 - V_1/n)/L \times (t_5 - t_4). \tag{12}$$

The turn-on of switches S_6 and S_7 in HV side bridge. In the LV side bridge, X and S_3 switches turn on during the time interval from t_5 to t_6 as depicted in Figure 8(f). HV Side and LV side voltages are V_1 and $V_2/2$ respectively. Current i_L decreases and is expressed as,

$$i_L(t) = i_L(t_5) + (V_2/2 - V_1/n)/L \times (t_6 - t_5). \tag{13}$$

The turn-on of switches S_6 and S_7 in HV side bridge. In the LV side bridge, S_2 and S_4 switches turn on during the time interval from t_6 to t_7 as depicted in Figure 8(g). HV Side and LV side voltages are V_1 and 0 respectively. Current i_L decreases and is expressed as,

$$i_L(t) = i_L(t_6) - (V_1)/nL \times (t_7 - t_6). \tag{14}$$

Furthermore, for reverse mode of operation the switching states as shown in Table 4 and has been carried out in accordance with the aforementioned operation.

Table 3 States of switches of proposed FLDAB converter using PSO based modulation for forward mode of operation

Switching States	Modes													
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
S_1	1	0	1	1	0	0	0	0	0	0	0	0	0	1
S_2	0	0	0	0	0	0	1	1	0	1	1	0	0	0
S_3	1	0	0	0	0	0	0	0	1	1	1	1	1	1
S_4	0	1	1	1	1	1	1	1	0	0	0	0	0	0
S_5	1	1	1	1	1	0	0	0	0	0	0	0	1	1
S_6	0	0	0	0	0	1	1	1	1	1	1	1	0	0
S_7	0	0	0	1	1	1	1	1	1	1	0	0	0	0
S_8	1	1	1	0	0	0	0	0	0	0	1	1	1	1
X_1	0	0	0	0	0	0	0	0	1	0	0	1	1	0
X_2	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Table 4 States of switches of proposed FLDAB converter using PSO based modulation for reverse mode of operation

Switching States	Modes													
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
S_1	1	0	0	0	0	0	0	0	0	0	1	1	0	1
S_2	0	0	0	1	1	0	1	1	0	0	0	0	0	0
S_3	1	1	1	1	1	1	0	0	0	0	0	0	0	0
S_4	0	0	0	0	0	0	1	1	1	1	1	1	1	0
S_5	1	1	0	0	0	0	0	0	0	1	1	1	1	1
S_6	0	0	1	1	1	1	1	1	1	0	0	0	0	0
S_7	0	0	0	0	1	1	1	1	1	1	1	0	0	0
S_8	1	1	1	1	0	0	0	0	0	0	0	1	1	1
X_1	0	1	1	0	0	1	0	0	0	0	0	0	0	0
X_2	0	0	0	0	0	0	0	0	1	1	0	0	1	0

5.2 Harmonic Approach with PSO-Algorithm for Improved System Performance

Significant power loss in a system is attributed to harmonics, which are signals characterized by frequencies that are integer multiples of the fundamental frequency. The mitigation of harmonic content in inductor current is crucial due to its potential to decrease losses in high-frequency transformer (HFT), which play a vital role in the operation of the multi-level dual active bridge (MLDAB) system. The utilization of the Fourier series methodology offers a comprehensive equations. The voltage waveform denoted as v_{hv} has a square shape with three distinct levels and possesses the property of

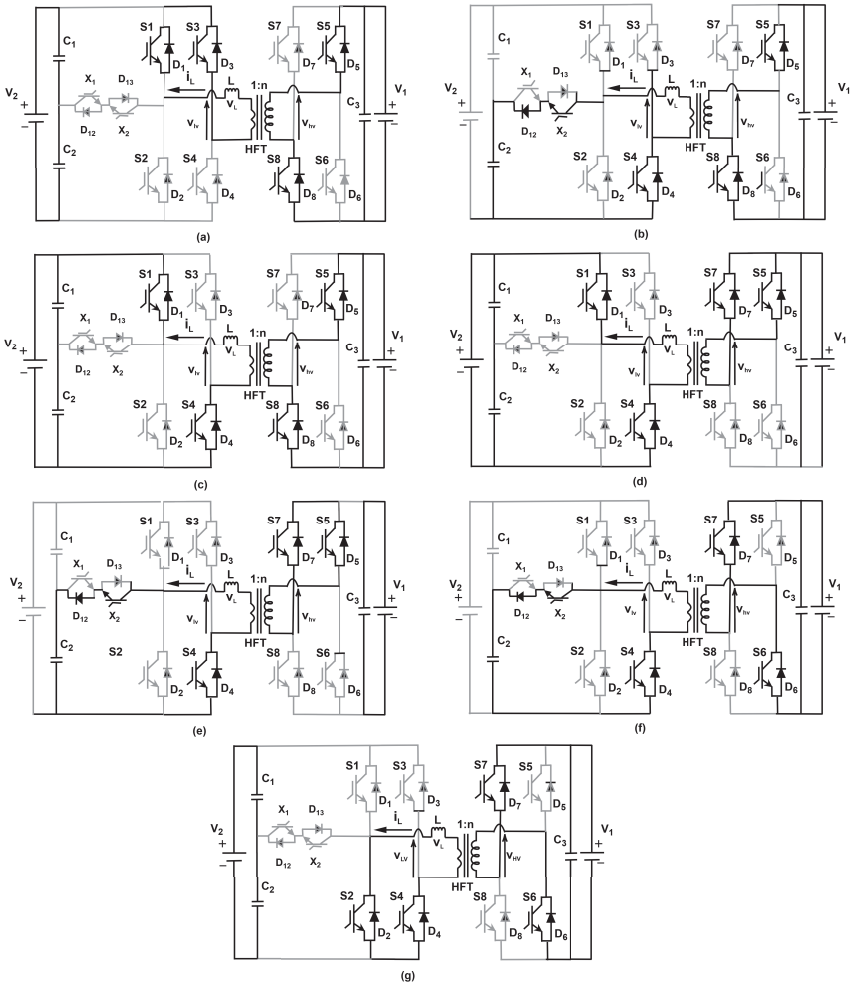

Figure 7 G2V operation of proposed modulation based FLDAB converter, whereas a) $t_0 - t_1$, b) $t_1 - t_2$, c) $t_2 - t_3$, d) $t_3 - t_4$, e) $t_4 - t_5$, f) $t_5 - t_6$ and g) $t_6 - t_7$.

half-wave symmetry as shown in Figure 6. Because of the principle of half-wave symmetry, the coefficient a_0 is determined to be zero. Additionally, the coefficients a_n and b_n are also zero for values of n that are even. Consequently,

$$v_{hv}(t) = \sum_{n=1}^{\infty} (a_n cos(n\omega_o t) + b_n sin(n\omega_o t)) \tag{15}$$

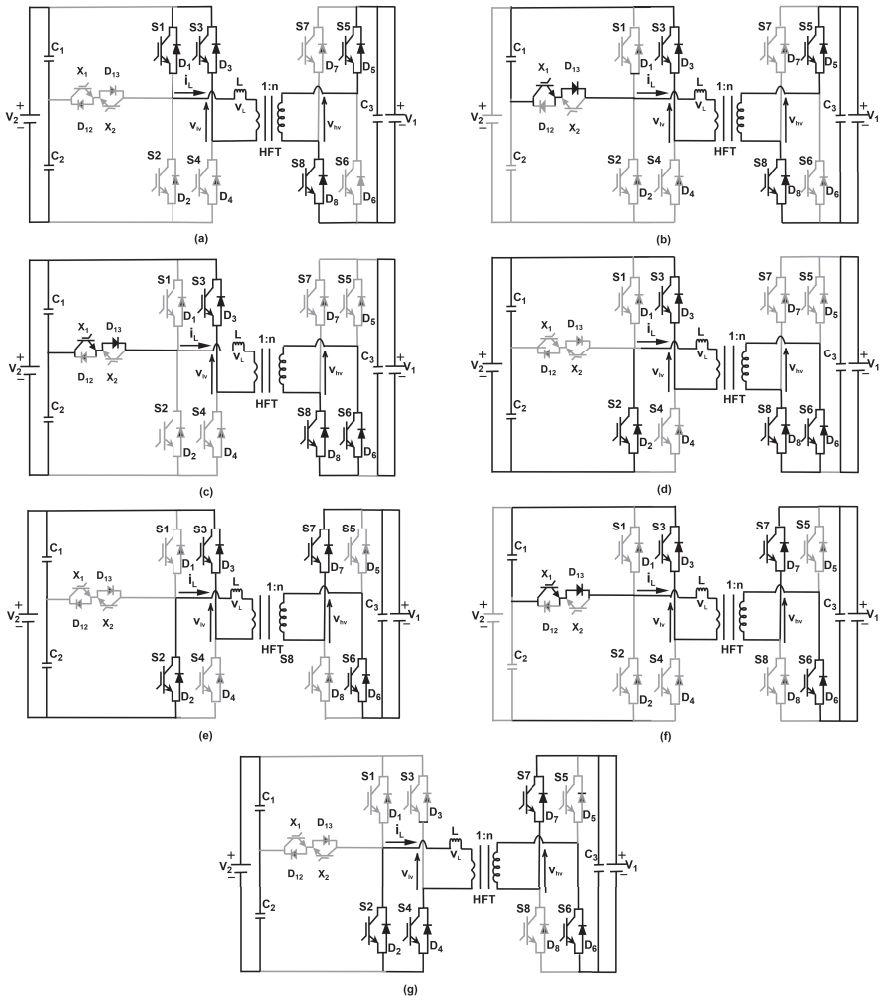

Figure 8 V2G operation of proposed modulation based FLDAB converter, whereas a) $t_0 - t_1$, b) $t_1 - t_2$, c) $t_2 - t_3$, d) $t_3 - t_4$, e) $t_4 - t_5$, f) $t_5 - t_6$ and g) $t_6 - t_7$.

where;

$$a_n = \frac{4}{T}\int_0^{T/2} v_{hv}(t)cosn(\omega tdt$$

$$b_n = \frac{4}{T}\int_0^{T/2} v_{hv}(t)sinn(\omega tdt$$

From Figure 6, v_{hv} is 0 for the time interval πd_4 and is V_1 for $\pi(1-d_4)$. Thus, on solving (15),

$$v_{hv}(t) = \sum_{n=1,3,5}^{\infty} \frac{2v_1}{n\pi} \times \sqrt{2 \times (1+\cos(nd_4))} \times \sin(n\omega_0 t - nd + \varphi)$$

$$\tan(\varphi) = -\frac{\sin(nd_4)}{1+\cos(nd_4)} \tag{16}$$

Likewise, the variable v_{lv} represents a square waveform consisting of five levels, exhibiting both odd and half-wave symmetry. Therefore, the values of $\mathrm{a_0}$ and $\mathrm{a_n}$ are both equal to 0 for all values of n, whereas the value of $\mathrm{b_n}$ is equal to 0 only for even values of n and can be written as;

$$v_{lv}(t) = \sum_{n=1,3,5\ldots}^{\infty} b_n \sin(nw_0 t) \tag{17}$$

where;

$$b_n = \frac{8}{T}\int_0^{T/4} v_{lv}(t)\sin n\omega t dt$$

From Figure 6, v_{lv} is 0 for time interval πd_1; $V_2/2$ for πd_2 and V_2 for πd_3. Thus, on solving (17),

$$v_{lv}(t) = \sum_{n=1,3,5..}^{\infty} \frac{2V_2}{n\pi}\lambda \sin(n\omega_0 t) \tag{18}$$

where;

$$\lambda = \cos(n\pi(d_1+d_2)) + 2\cos(n\pi d_1) - \cos(n\pi(d_1+d_2+2d_3))$$

The inductor voltage is given as;

$$v_L = v_{lv} - kv_{hv} \tag{19}$$

By performing integration, the expression for the inductor current as below;

$$i_L = \frac{1}{L}\int_0^t v_L + i(0) \tag{20}$$

As the average inductor current throughout a switching time is zero, it can be deduced that the inductor current at π/ω_0 is equivalent to $-\mathrm{i}(0)$. By

evaluating the expression $\mathrm{i}(0)$, it is possible to determine the current flowing through the inductor using equation (20).

$$i_L = \sum_{n=1,3,5..}^{\infty} \frac{2}{n^2\omega_0\pi L} \times \sqrt{A^2+B^2} \times \sin\left(n\omega_0 t + \theta\right) \tag{21}$$

where,

$$A = 2V_1 \cos\left(n\left(d+\frac{d_4}{2}\right)\right)\cos\left(n\frac{d_4}{2}\right) - kV_2\lambda$$

$$B = 2V_1 \sin\left(n\left(d+\frac{d_4}{2}\right)\right)\cos\left(n\frac{d_4}{2}\right)$$

$$\tan(\theta) = \frac{A}{B}$$

From equation (21), the RMS current $i_L(rms)$ is represented as;

$$i_{L(rms)} = \sqrt{\sum_{n=1,3,5..}^{\infty} \left(\frac{\sqrt{2}}{n^2\omega_0\pi L} \times \sqrt{A^2+B^2}\right)^2} \tag{22}$$

Harmonics cause significant power loss in the system. It is crucial to lower the harmonic content of inductor current, since doing so can lower HFT losses, which is an important component of the MLDAB. In order to seek a set of optimal operating points to reduce system loss and improve the efficiency of the DAB converter, PSO algorithm is adopted for system optimization. The rms inductor current, which is adopted as the objective function and finding a set of optimal combination of $(d_1\pi, d_2\pi, d_3\pi, d_4\pi, d\pi)$ to minimize the rms inductor current under constraints based on the operational principle of the proposed MLDAB converter are shown as follows;

$$\begin{cases} (d_1+d_2+d_3)\pi = 0.5\pi \\ d_1\pi \in [0, \pi/2] \\ d_2\pi \in [0, \pi/2] \\ d_3\pi \in [0, \pi/2] \\ d_4\pi \in [0, \pi/2] \\ d\pi \in [-\pi, \pi] \end{cases} \tag{23}$$

Figure 9 illustrates the optimization flowchart. In the start stage, constraints as in equation (23), for the fitness function as in equation (22). After that, the PSO algorithm will conduct fitness evaluation, then update P_{best}

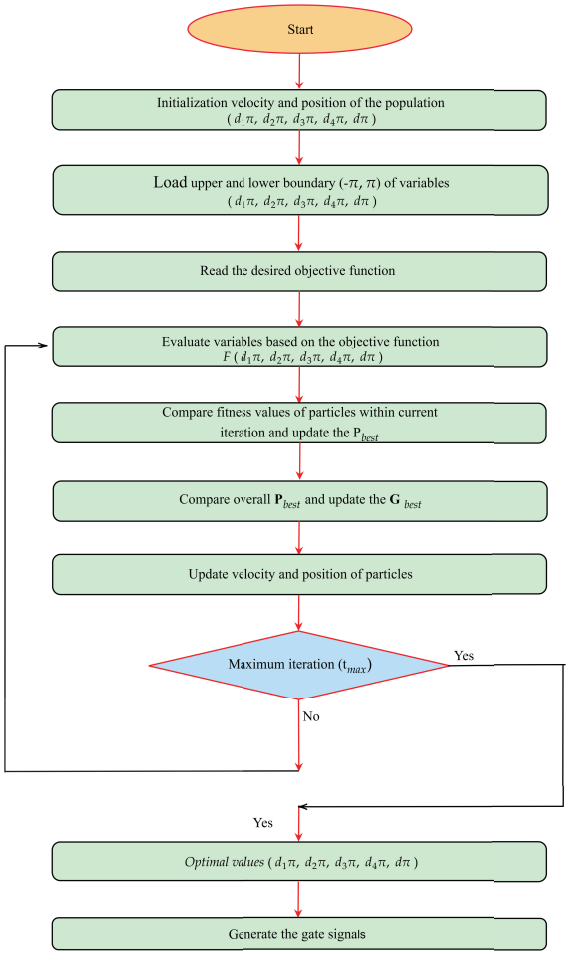

Figure 9 Flowchart of the proposed PSO algorithm.

and G_{best} as well as the velocity and position of particles. The termination condition for the PSO algorithm is based on the criteria. If the maximum iteration is reached. The system achieves the minimum RMS current. After that, optimal variables ($d_1\pi, d_2\pi, d_3\pi, d_4\pi, d\pi$) are obtained and gate signals are generated.

PSO algorithm, in addition to its outstanding global search ability, it also features the merits of good robustness and fast computation speed and it is adopted in this article. The PSO algorithm mimics the random hunting behavior of birds. It first needs to initialize a swarm of randomly distributed

particles in the n-dimensional search space. For the optimization problem in this article, since the position of each particle is determined by the combination of (d_1, d_2, d_3, d_4, d). Each individual particle represents a potential optimal solution, which involves two characteristic indexes, position X and velocity V.

$$X_i = (X_{i1}, X_{i2}, X_{i3}, X_{i4}, X_{i5})$$
$$V_i = (V_{i1}, V_{i2}, V_{i3}, V_{i4}, V_{i5})$$

where the initial number of particles is defined as X_i and V_i are the position and velocity of the i-th particle, respectively. The key of the PSO algorithm is the updating formulas of velocity and position for each individual particle.

$$\begin{cases} V_i^{m+1} = \omega V_i^m + c_1 r_1 (\text{Pxbest}_i^m - X_i^m) + c_2 r_2 (\text{Gxbest}^m - X_i^m) \\ X_i^{m+1} = X_i^m + V_i^{m+1} \end{cases}$$

where;

- m is the iteration index.
- ω is the inertia weight, generally $\omega = 0.5$–1, reflecting the tendency of a particle to maintain its previous velocity.
- c_1 is the individual learning factor, generally 0–4. It reflects the tendency of a particle to approach the historical optimal position of individual Pxbest.
- c_2 is the swarm learning factor, generally 0–4. It reflects the tendency of particles to approach the historical optimal position of swarm Gxbest.
- r_1 and r_2 are randomly generated numbers, generally 0–1.

It is after countless iterations that the particle can successfully reach the position with the optimal fitness value, which is exactly the optimal solution to the optimization problem. As shown below, the generalized PSO Pseudo-Code is as follows.

Step 1: Initialize constants: Set the values of k, ω_0, L, and N.

Step 2: Initialize PSO parameters: Define the particle swarm optimization parameters:

- `population_size`
- `max_iterations`
- `inertia_weight` (w)
- `cognitive_component` (c_1)
- `social_component` (c_2)

Step 3: Set bounds for decision variables:

$$d_1, d_2, d_3, d_4 \in [0, 0.5], \quad d_5 \in [-1, 1]$$

Step 4: Initialize particles:

- Randomly assign d_1, d_2, d_3 such that $d_1 + d_2 + d_3 = 0.5$
- Randomly assign $d_4 \in [0, 0.5]$ and $d_5 \in [-1, 1]$
- Initialize velocities randomly
- Set `pbest` = position, `pbest_fitness` = ∞
- Set `gbest` = None, `gbest_fitness` = ∞

Step 5: Repeat for each iteration (1 to max_iterations):

Step 6: For each particle i in the swarm:

1. Extract d_1, d_2, d_3, d_4, d_5
2. If $d_1 + d_2 + d_3 \neq 0.5$, normalize:

$$\text{total} = d_1 + d_2 + d_3$$

$$d_1 = \frac{d_1}{\text{total}} \cdot 0.5, \quad d_2 = \frac{d_2}{\text{total}} \cdot 0.5, \quad d_3 = \frac{d_3}{\text{total}} \cdot 0.5$$

3. Clip values:

$$d_1, d_2, d_3, d_4 \in [0, 0.5], \quad d_5 \in [-1, 1]$$

4. Evaluate fitness using `fitness_function`$(d_1, d_2, d_3, d_4, d_5)$
5. If fitness $<$ `pbest_fitness`, update `pbest` and `pbest_fitness`

Step 7: Update `gbest` as the best among all `pbest` values.

Step 8: Display current best fitness and corresponding $(d_1, d_2, d_3, d_4, d_5)$.

Step 9: For each particle i:

1. Update velocity:

$$v = w \cdot v + c_1 \cdot r_1 \cdot (\text{pbest} - x) + c_2 \cdot r_2 \cdot (\text{gbest} - x)$$

2. Update position: $x = x + v$
3. Clip values to bounds:

$$d_1, d_2, d_3, d_4 \in [0, 0.5], \quad d_5 \in [-1, 1]$$

4. Renormalize $d_1 + d_2 + d_3 = 0.5$ (as in Step 6.2)

Step 10: Return `gbest` and its fitness.

5.3 Efficiency and Loss Estimation

Losses in the converter mostly occur in switches and transformer. In switches, conduction and switching losses are taken into account [28, 29], whereas in high frequency transformer, core losses and conduction losses are considered [30, 31].

5.3.1 Losses in switches

Lets, I_{sw} is the RMS current through switches, R_{on} is the on state resistance, V_{on} is the switch voltage before turn on, V_{off} is the switch voltage after turn off, t_{on}, t_{off} are the turn on delay and turn off delay time respectively, i_{on} is the current after switch turn on, i_{off} is the current before switch turn off, then conduction losses through switches are given as,

$$P_{con} = I_{sw}^2 \times R_{on}. \tag{24}$$

$$P_{dcon} = I_D \times V_f. \tag{25}$$

And the switching losses are given as,

$$\begin{aligned} P_{sw} &= \text{Turn on switching loss + Turn off switching losses} \\ P_{sw} &= 1/2[V_{on} \times i_{on} \times t_{on} + V_{off} \times i_{off} \times t_{off}] \times f. \\ &= [E_{on} + E_{off}] \times f. \end{aligned} \tag{26}$$

Hence the total losses in switches are as,

$$P_T = P_{con} + P_{sw}$$

5.3.2 Losses in high frequency transformer

Let I_{pri} and I_{sec} are the RMS current through primary and secondary winding, R_w is the winding resistance, W_{tfe} is the core weight, B_{ac} is the magnetic flux density. The losses in the high frequency transformer can be calculated as the primary side conduction loss as below,

$$P_{cu1} = I_{pri}^2 \times R_w$$

and the secondary side conduction loss as,

$$P_{cu2} = I_{sec}^2 \times Rw$$

Also the core losses as shown below,

$$Pfe(W) = P_{fe}(mW/g) \times W_{tfe} \times 10^{-3} \tag{27}$$

Table 5 System specifications

Parameters	**Values**
Switching frequency (f_s)	$20\,kHz$
HFL-inductor (L)	$151\,\mu H$
Voltage at DC link (V_{dc})	$650\,V$
Nominal battery voltage (V_{bat})	$500\,V$
Rated battery capacity (Ah)	$250\,Ah$
Turns ratio (n)	1.3

Finally the total losses in HFT as shown below,

$$P_{cu1} + P_{cu2} + P_{fe}$$

Therefore the total losses in converter = Total Losses in Switches + Total Losses in HFT.

5.3.3 Efficiency calculation

$$\eta = \frac{Output}{(TotalLosses + Output)} \times 100 \tag{28}$$

The comparison of the proposed MLDAB based converter has been done with the conventional SPS, EPS, DPS, TPS and QPS mdoulation based DAB converters [26, 27]. The comparison shows substantial decrease in the inductor current THD (%), results in more efficiency of the proposed converter compared to other conventional converters as mentioned in the Table 6 and Figure 24.

6 Results

6.1 Simulation Results

The parameters and their corresponding values used for simulating the conventional and proposed systems are detailed in Table 5.

6.1.1 Simulation Outcomes of Conventional FLDAB Converter Employing QPS Modulation

Figure 10(a–d) comprehensively illustrates the steady-state G2V performance of the conventional FLDAB converter utilizing QPS modulation. Figures 10(b) and 10(a) depict the voltage waveforms at the LV and HV sides respectively, showcasing the voltage profiles generated by the modulation

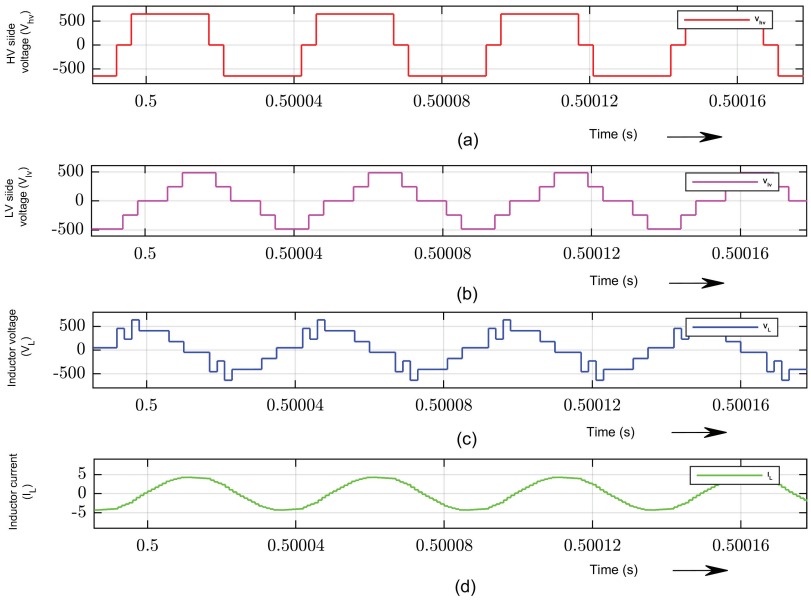

Figure 10 G2V performance evaluation of conventional MLDAB converter.

scheme. The inductor voltage as shown in Figure 10(c) and the behaviour of the inductor current is further detailed in Figure 10(d), where it increases and decreases when the voltage becomes positive and negative across the inductor respectively. This ensures a directional flow of current from the grid to the vehicle (G2V) of the FLDAB converter.

Figure 11(a—d) illustrates the V2G operational characteristics of the MLDAB converter. Figures 11(b) and 11(a) present the voltage waveforms at the LV and HV sides respectively, highlighting the distinct voltage patterns achieved through the modulation scheme. The inductor voltage is a result of the difference between voltages as presented in Figure 11(c). The behaviour of the inductor current, as elaborated in Figure 11(d), shows a characteristic rise when the voltage across the inductor is positive and a decline during negative voltage intervals. This controlled variation facilitates the flow of current from the vehicle to the grid (V2G), thereby ensuring efficient and seamless power transfer within the system.

To substantiate the efficacy of the conventional FLDAB converter, the study conducts a comprehensive analysis for varying external phase shift ratios, d. Encapsulation of the inductor current profile alongside their respective Total Harmonic Distortion (THD) spectra across a spectrum of d values

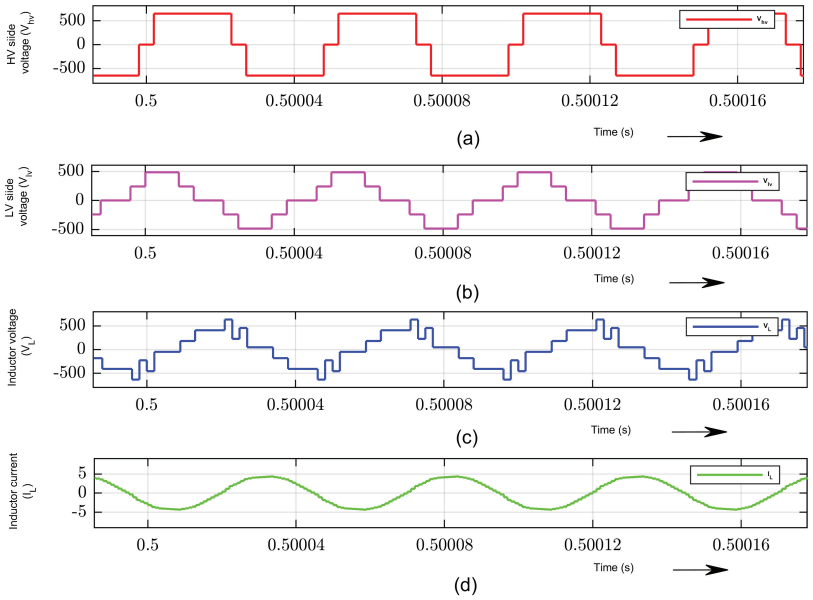

Figure 11 V2G performance evaluation of conventional MLDAB converter.

is shown in Figure 12(a—l). The study adopts a uniform internal modulation index configuration $(d_1 = d_2 = d_3 = d_4)$ fixed at 0.17, while systematically varying the (d). The resulting THD percentages are determined to be 5.16, 4.85, 4.58, 4.64, 4.70 and 4.99.

6.1.2 Simulation outcomes of proposed FLDAB converter using PSO algorithm based modulation

Figure 13(a—d) comprehensively illustrates the steady-state G2V performance of the proposed MLDAB converter with PSO based modulation. Figures 13(b) and 13(a) depict the voltage waveforms at the LV and HV sides respectively, showcasing the voltage profiles generated by the modulation scheme. The inductor voltage is a result of the difference between voltages as presented in Figure 13(c). The behaviour of the inductor current as elaborated in Figure 13(d), shows a characteristic rise when the voltage across the inductor is positive and a decline during negative voltage intervals. This ensures a flow of current from the grid to the vehicle (G2V) of the MLDAB converter.

Figure 14(a–d) illustrates the V2G operational characteristics. Figures 14(b) and 14(a) present the voltage waveforms at the LV and HV sides

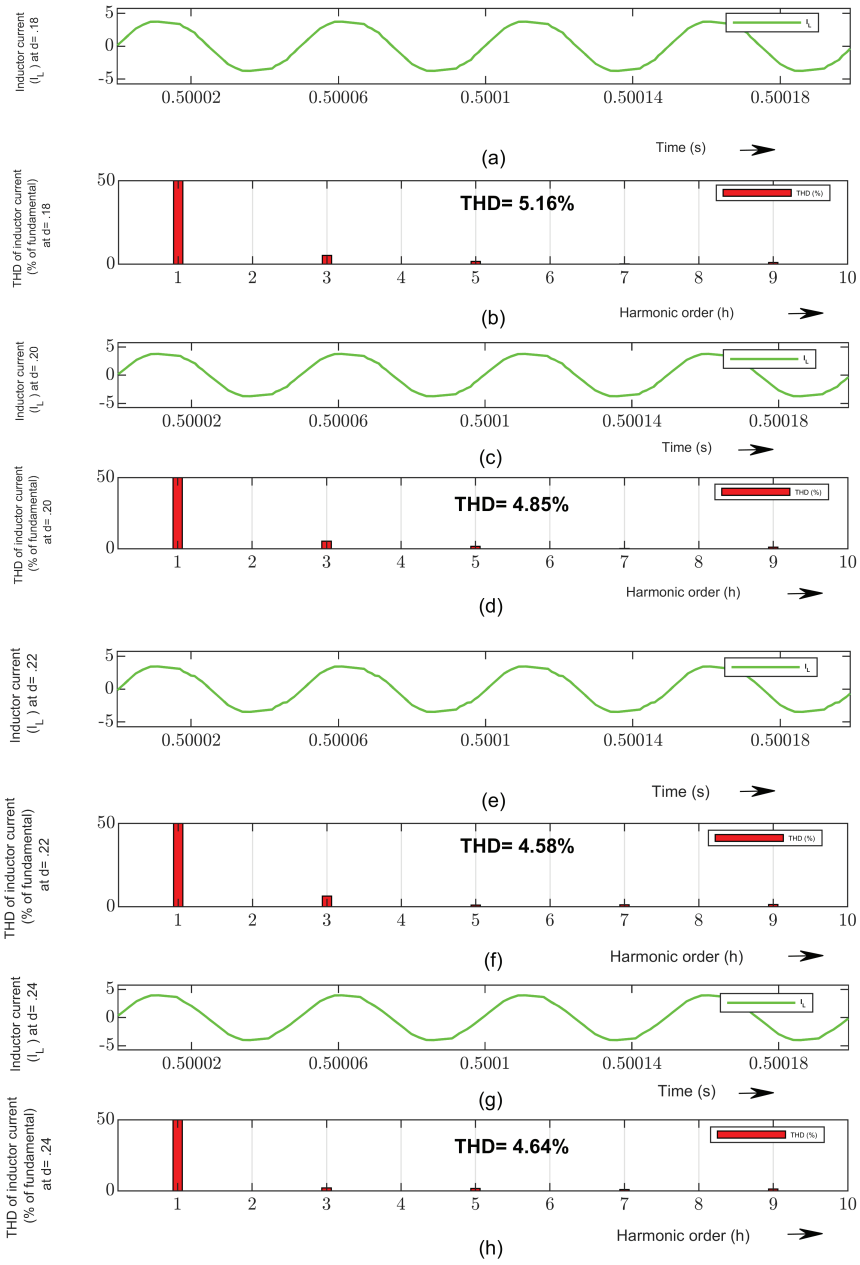

Figure 12 Continued

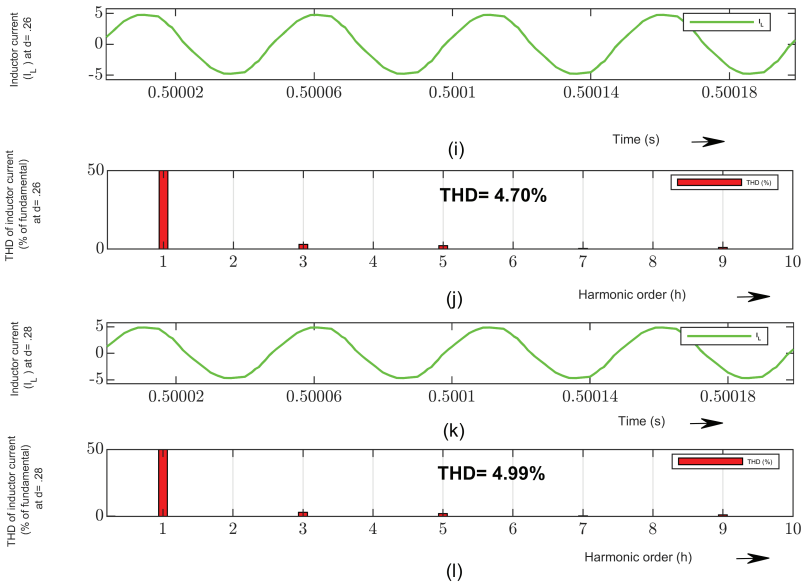

Figure 12 At different values of d performance evaluation of conventional MLDAB converter.

respectively, highlighting the distinct voltage patterns achieved through the modulation scheme. The result of the voltage difference results in inductor voltage as in Figure 14(c). The behaviour of the inductor current as elaborated in Figure 14(d), shows a characteristic rise when the voltage across the inductor is positive and a decline during negative voltage intervals. This controlled variation facilitates the flow of current from the vehicle to the grid (V2G) of the MLDAB converter, thereby ensuring efficient and seamless power transfer within the system.

The study adopts a uniform internal modulation index configuration $(d_1 = d_2 = d_3 = d_4)$ fixed at 0.167, while systematically varying the external phase shift ratio (d). The resulting THD percentages for these corresponding parameter variations are determined to be 3.96, 3.63, 3.31, 3.39, 3.42 and 3.69 thereby to justify the proposed modulation strategy. The operational framework considers the internal modulation index ratios $(d_1 = d_2 = d_3 = d_4)$ assigned a value of 0.167, in conjunction with (d) fixed at 0.22. This particular set of parameters represents the optimal configuration derived through the application of the Particle Swarm Optimization (PSO) algorithm. The objective of this optimization is to systematically minimize

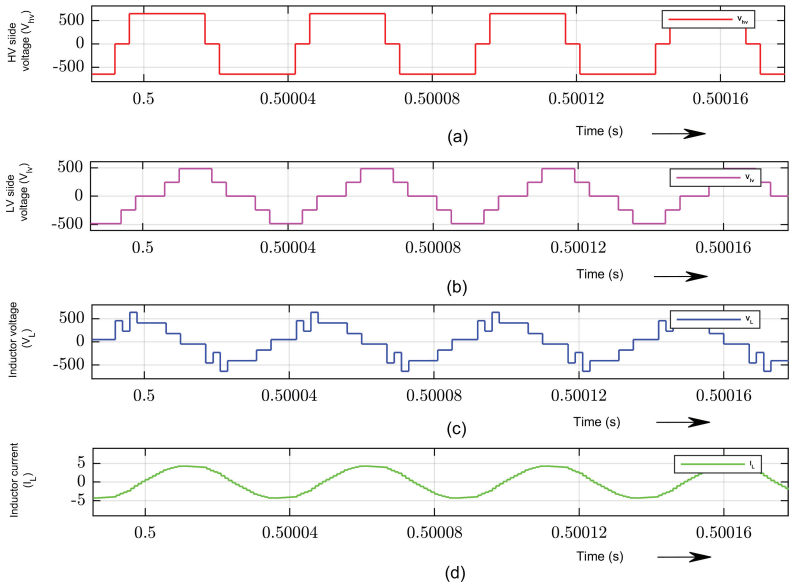

Figure 13 G2V performance evaluation of proposed MLDAB converter.

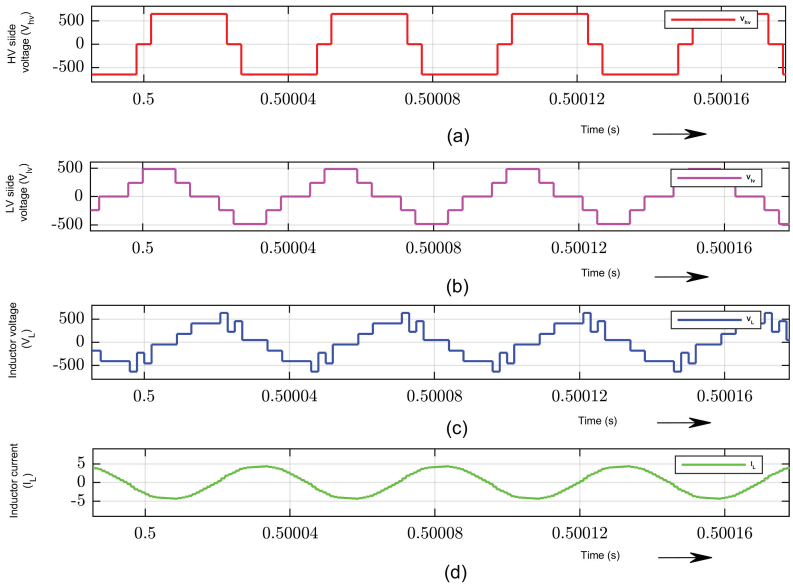

Figure 14 V2G performance evaluation of proposed MLDAB converter.

inherent system losses while concurrently enhancing the overall efficiency of the proposed converter, thereby achieving superior performance metrics within the defined operational limits.

6.2 Real Time Results

Here the validation of results using the setup as shown in Figure 16, consist of OPAL-RT (OP4510), power quality analyser, digital signal oscilloscope, and a desktop computer.

6.2.1 Real time outcomes of conventional MLDAB converter employing QPS modulation

Figure 17(a—b) illustrates the Real-time performance metrics of the conventional converter operating in the forward mode. The difference in voltage corresponding to the voltage across the inductor as in Figure 17(a). Additionally, the Total Harmonic Distortion (THD) of the inductor current during the G2V operation is recorded at 4.70%, as in Figure 17(b) indicating the quality of current waveform under these conditions.

Figure 18(a—b) illustrates the Real-time performance metrics operating in the V2G mode. The voltage difference corresponding to the voltage across the inductor as in Figure 18(a). Additionally, the Total Harmonic Distortion (THD) of the inductor current during the V2G operation is recorded at 4.80%, as in Figure 18(b), indicating the quality of current waveform under these conditions.

Furthermore, this study conducts a comprehensive analysis for varying external phase shift ratios d. Figure 19(a—f) encapsulates the inductor current profiles alongside their respective THD spectra across a spectrum of d values. The study adopts a uniform internal modulation index configuration $(d_1 = d_2 = d_3 = d_4)$ fixed at 0.17, and while systematically varying the external phase shift ratio (d). The resulting THD percentages corresponding to these parameter variations are determined to be 4.80, 4.50, 4.30, 4.40, 4.40 and 4.70 respectively.

6.2.2 Real time outcomes of proposed MLDAB converter using PSO algorithm based modulation

Figure 20(a—b) illustrates the real-time performance metrics of the proposed FLDAB converter operating in the forward mode. The difference in voltage corresponding to the voltage across the inductor as in Figure 20(a). Additionally, the Total Harmonic Distortion (THD) of the inductor current during the

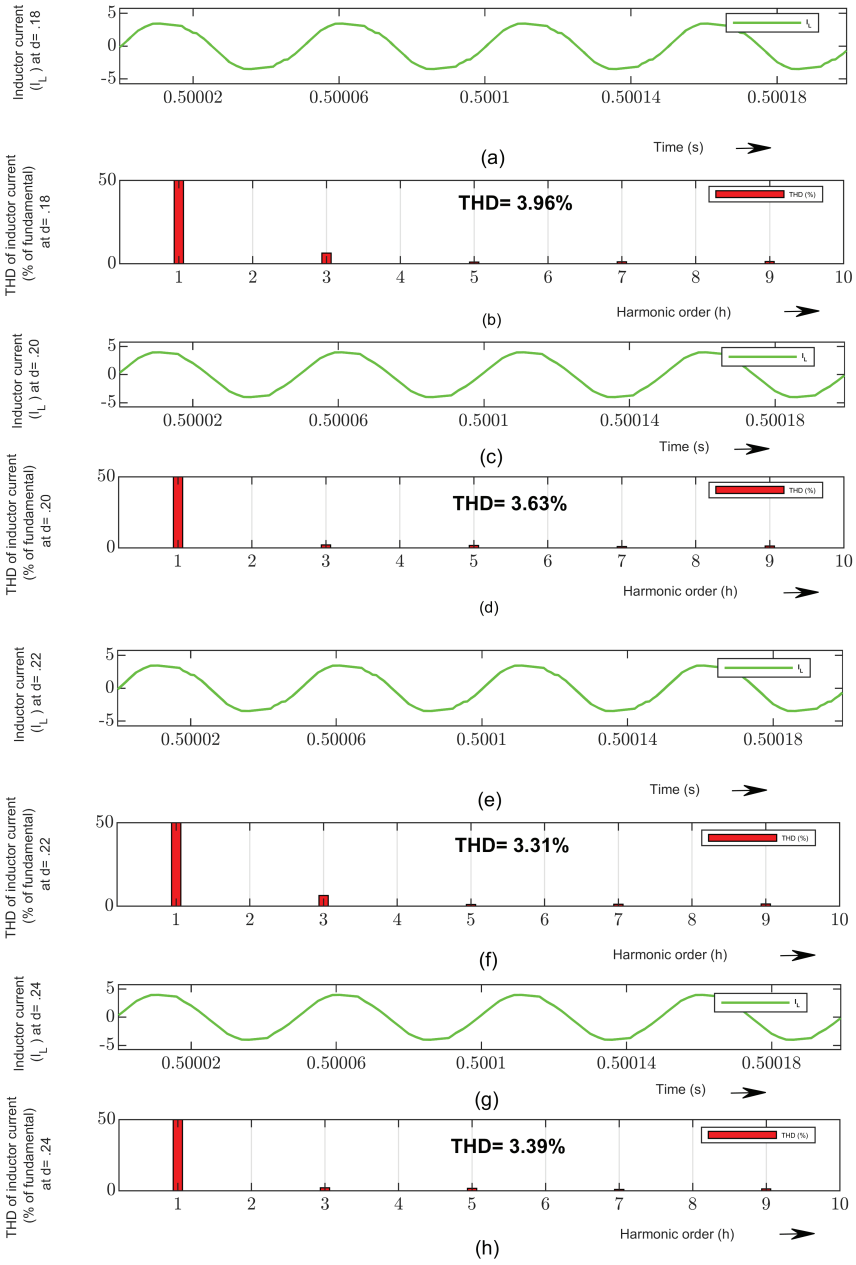

Figure 15 Continued

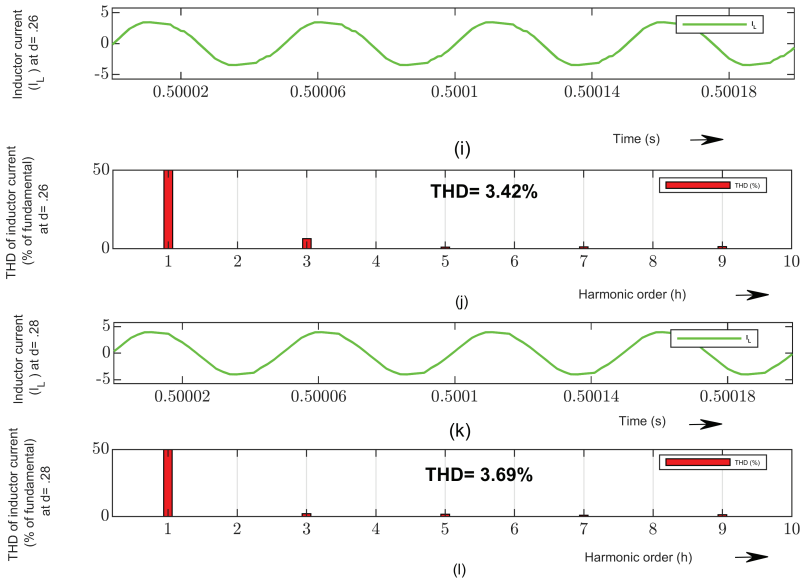

Figure 15 At different values of d performance evaluation of proposed converter.

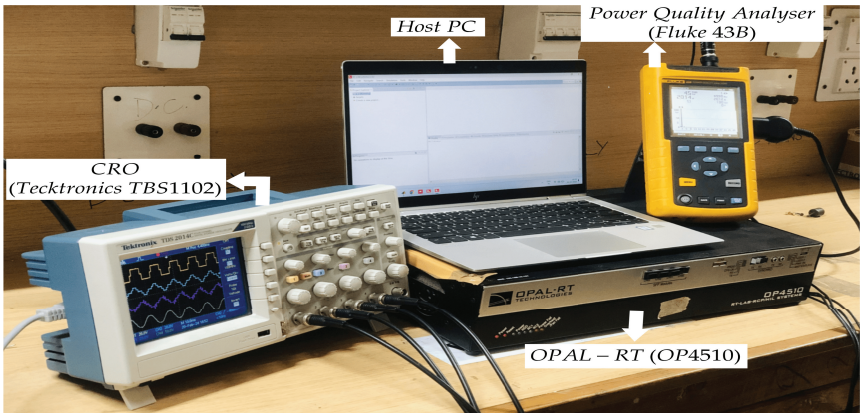

Figure 16 The setup for the validation of the results pertaining to the MLDAB converter.

G2V operation is recorded at 3.10%, as in Figure 20(b) indicating the quality of current waveform under these conditions.

Figure 21 illustrates the real-time performance metrics operating in the V2G mode. The voltage difference corresponding to the voltage across the inductor as in Figure 21(a). Additionally, the Total Harmonic Distortion

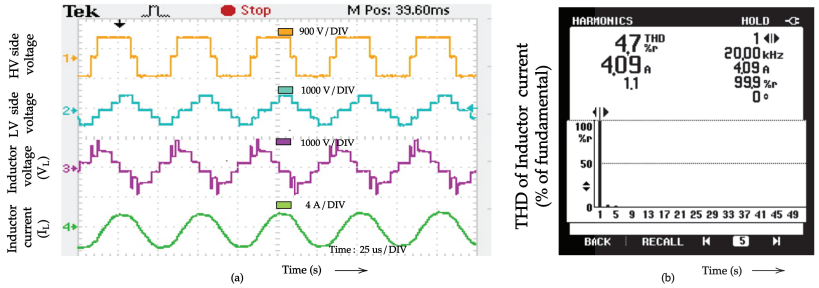

Figure 17 G2V real-time performance results.

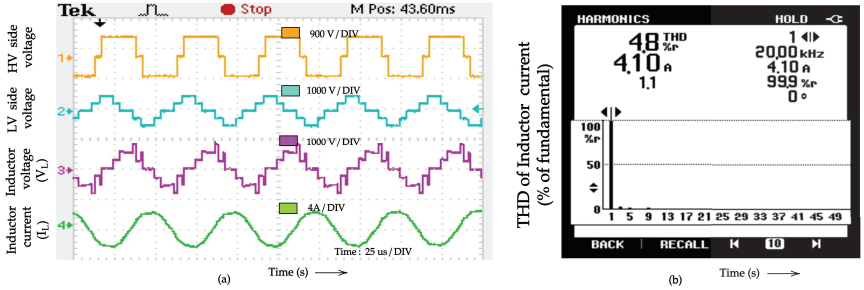

Figure 18 V2G real-time performance results.

(THD) of the inductor current during the V2G operation is recorded at 3.20%, as in Figure 21(b), indicating the quality of current waveform under these conditions.

Furthermore, this study conducts a comprehensive analysis for varying external phase shift ratios d. Figure 22(a—f) encapsulates the inductor current profiles alongside their respective THD spectra across a spectrum of d values. The study adopts a uniform internal modulation index configuration $(d_1 = d_2 = d_3 = d_4)$ fixed at 0.167, and while systematically varying the (d) as 0.18, 0.20, 0.22, 0.24, 0.26 and 0.28. The resulting THD percentages corresponding to these parameter variations are determined to be as 3.5 %, 3.2 %, 3.0 %, 3.1%, 3.2% and 3.4% respectively.

The analysis of the FFT plots clearly demonstrates reduction in the inductor current THD, thereby mitigating the associated heating effects. Furthermore, Figure 23 presents a comparative analysis of the THD of current across different values of d. The results unequivocally illustrate lower THD in comparison to the conventional MLDAB converter, thereby indicating a superior harmonic performance and enhanced operational efficiency.

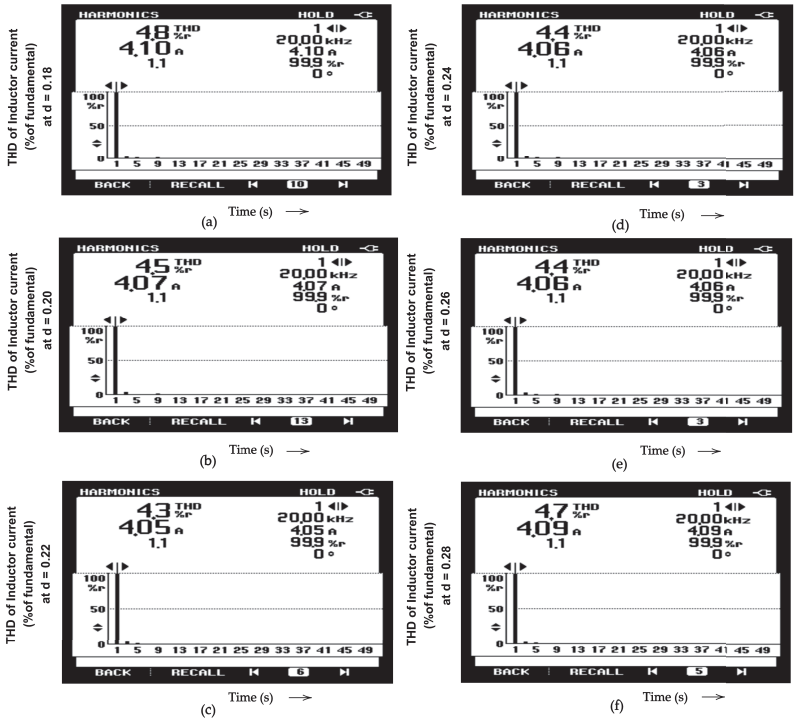

Figure 19 At different values of d, real time results related to harmonic analysis of inductor current.

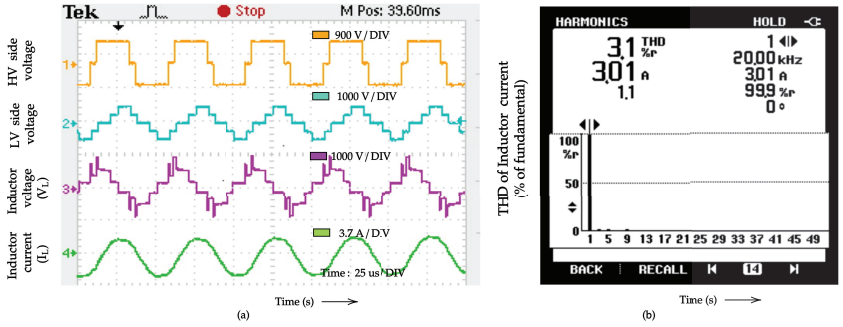

Figure 20 G2V real-time performance results of the proposed converter.

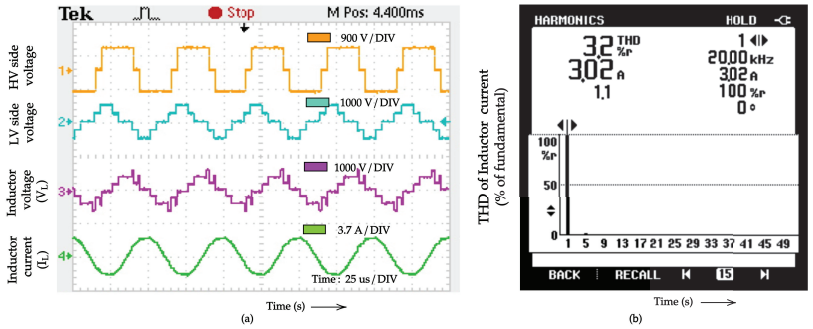

Figure 21 V2G real-time performance of the proposed converter.

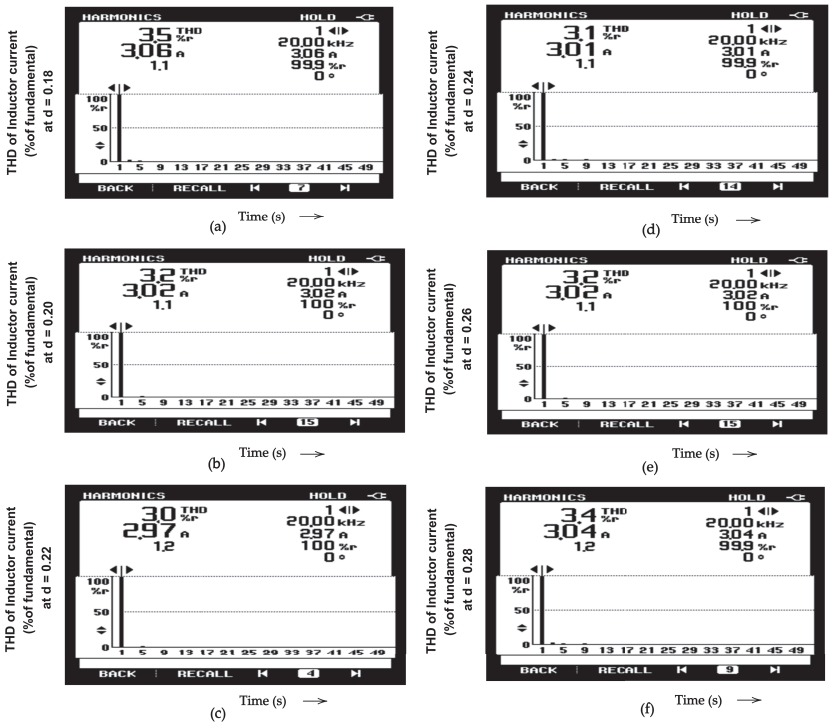

Figure 22 At different values of *d*, real time results related to harmonic analysis of inductor current.

7 Performance Comparison

This study carries out a comparative analysis to assess the performance enhancements of the proposed MLDAB converter harnessing PSO based

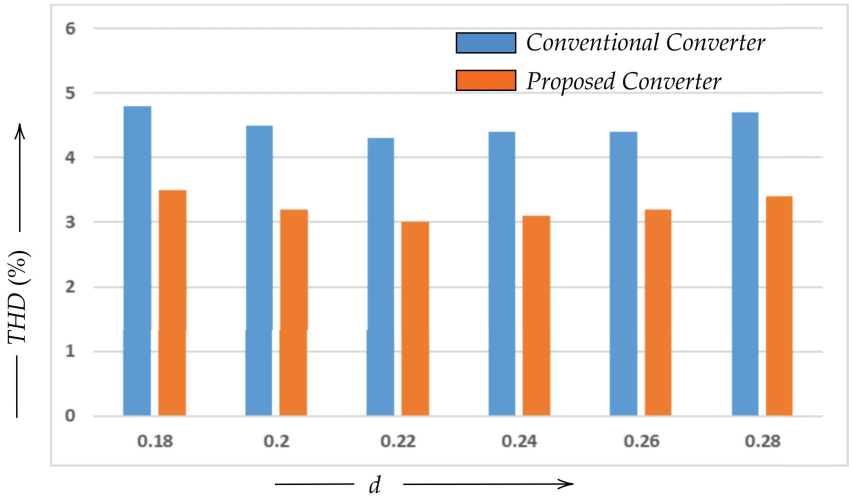

Figure 23 THD (%) plot assessment for different d values.

Table 6 Comparative analysis.

Parameters	Voltage Level	Degrees of Freedom (DOF)	No. of (Switches + Diodes)	THD (%)	Efficiency (%)
SPS based DAB Converter [26]	1	2	8	17.54	88.78
EPS based DAB Converter[26]	2	3	8	16.58	91.08
DPS based DAB Converter [26]	2	3	8	7.60	91.20
TPS based DAB Converter [26]	3	3	8	5.28	91.28
QPS based MLDAB Converter[27]	5	5	9 + 4	4.30	95.50
Proposed MLDAB Converter	5	5	10	3.00	98.00

phase shift modulation. The findings indicate that harmonics is lower than that of the conventional MLDAB converter as depicted in Figure 23. Furthermore, the proposed converter achieves improved efficiency, as illustrated in Table 6 for a power rating of 1kW and for different power ratings as shown in Figure 24, demonstrating its superior performance.

The proposed MLDAB converter topology, leveraging a PSO-based modulation scheme, achieves a five-level output with a minimized component count, thereby optimizing the overall efficiency. In contrast to the conventional converter, which necessitates four diodes for operation, the proposed MLDAB converter employs a single strategically placed active switch, thereby obviating the need for multiple components. This reconfiguration not only includes a considerable reduction in component count but also a substantial decrement in the overall system cost, thus reinforcing its economic viability without compromising performance metrics.

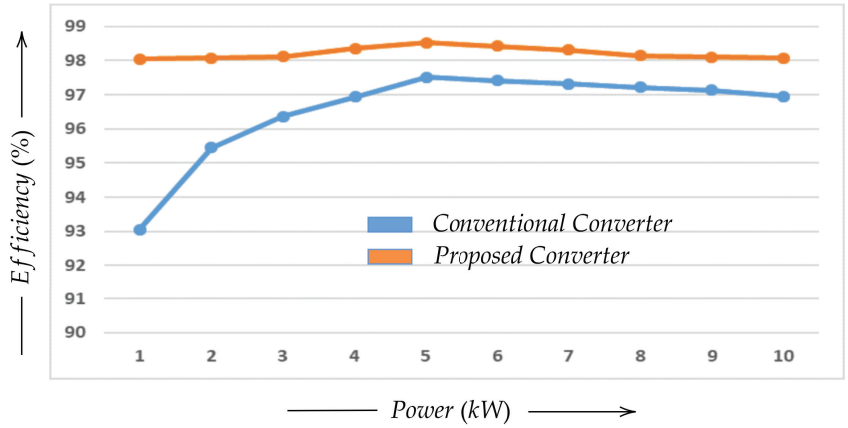

Figure 24 Efficiency assessment for different power ratings.

Furthermore, an examination of the conventional topology reveals that the current conduction trajectory involves an active switch in series with two diodes, as delineated in Figures 2 and 3. Conversely, the suggested topology redefines the operational conduction path, wherein the same functionality is realized exclusively by an active switch and a single diode, as illustrated in Figures 7 and 8. This redistribution of switching elements significantly alleviates the inherent circuital complexity while simultaneously augmenting the system's operational resilience.

Moreover, the implications of harmonic distortions in the HFL inductor current manifest in increased root-mean-square (RMS) current, which in turn results in a pronounced escalation in harmonics, results in excessive thermal stress within the system components, thereby imposing severe constraints on the overall system efficiency and long-term operational integrity. However, the integration of the PSO-driven modulation scheme within the proposed topology yield a profound attenuation of harmonic distortions, facilitating a near-sinusoidal inductor current profile. This sinusoidal current waveform significantly mitigates thermal accumulation within the HFT, thereby prolonging its operational lifespan while concurrently diminishing maintenance and failure probabilities.

In culmination, the symbiotic interplay of reduced economic burden, enhanced circuital simplicity, and superior reliability to achieve a high-efficiency, low-harmonic operation within a optimized framework substantiates its viability as an indispensable alternative to conventional power conversion topologies.

8 Conclusion

This paper presents a novel five-level dual active bridge (FLDAB) converter topology using PSO based modulation technique. The proposed topology designed to reduce inductor current harmonics as well as reduced component count, thereby decreasing losses and improving the efficiency, resulting in the overall enhanced performance. This study develops and simulates the suggested MLDAB converter with PSO algorithm-based modulation within the MATLAB/Simulink environment. The analysis reveals that the proposed MLDAB converter produces a nearly sinusoidal HFL current waveform. Furthermore, the results have been compared with those obtained from the conventional converter and it shows that the proposed MLDAB converter achieves lower inductor current harmonics across a broad range of operating conditions, as well as the increased efficiency is achieved. The OPAL-RT emulator results further validate these findings.

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