Design and Implementation of a Secure and Accurate Electronic Voting Machine Using Verilog on Zynq FPGA

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Abstract

A Verilog-based EVM on a Zynq Board that may enhance the security, reliability, and transparency of voting will be designed and developed. Using the Zynq System-on-Chip platform, it contains an integrative on-chip structure of ARM processor and FPGA fabric, thereby providing robust hardware for processing votes with minimal errors. This HDL called Verilog will be used to program the vote counting logic, results to be displayed, and user interaction. The system has several security layers – voter authentication and validation of votes – which therefore ensures integrity. It also supports multiple candidates and can accommodate real-time updates of votes displayed. The programmable nature of the Zynq platform allows it to be scaled and adapted for future use in different types and configurations of elections. In addition, the hardware implementation utilized here reduces tampering and unauthorized access threats, one of the major concerns when doing procedures in an

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election. Testing and simulation results confirm that the system is accurate and can perform according to the standards set up. The project will stress the efficient application of embedded systems and digital design to real-world applications, especially mission-critical areas like voting.

Keywords: Electronic voting machine, Zynq Board, security, scalability, hardware-based implementation, voter authentication, vote validation.

1 Introduction

With the Zynq Board and Verilog, EVM can be proposed as an effective solution to improve the accuracy, reliability, and security of electronic voting systems. Electronic voting is destined to be an integral part of modern democratic processes; however, with its critical role in modern democratic processes comes a need for advanced and secure hardware solutions [1]. The main benefit of the Zynq-7000 All Programmable SoC is the integration of both ARM-based processing systems and FPGA fabric, allowing the platform to even accommodate complex hardware logic implementations in combination with software-based control systems. Using Verilog for the hardware description means the design is tightly controlled over the digital logic required to execute the voting processes, such as casting, tallying, and results display [2].

Systems built around microcontrollers have several disadvantages compared to the EVM implemented using the Zynq Board. Indeed, the most important advantage is the dynamic reconfiguration of the FPGA fabric, which gives the flexibility to alter voting logic and system functionality at runtime without changing the hardware [3]. In other words, this is very useful for adapting evolving voting protocols, security improvements, and feature additions. Besides, the dual-core ARM Cortex-A9 processor of the Zynq platform supports fast computation of the user interfaces, data storage, and communication with other devices, for example, a printer or central database, to enable safe data transfer of the voting [4].

The greatest factor to be considered in any electronic voting is security. This is usually achieved through the FPGA-based architecture in Zynq Board, which results in logic security, primarily due to its ability to segregate hardware from potential software threats. As a hardware description language, the Verilog can implement directly at the hardware level most cryptographic algorithms and protocols in a way that eliminates the possibility of tampering or hacking through software exploits [5]. The other protection of a system

comes from the encryption and authentication of its bitstream on the FPGA. Furthermore, Verilog being used allows the design to be modular and scalable, which makes future development of the interface with other security solutions easier, for instance, biometric authentication, or blockchain-based verification systems [6].

The EVM for Zynq Board encompasses those aspects when voting counts that refer to ease and transparency. All steps in the process will be guided using an intuitive interface with clear instructions and feedback to the voter. The system consists of double-voting proofs, an anonymous vote, and a real-time count. Results can be displayed directly on the screen or sent to a server to be processed there. Verilog is used here, so there is complete control over the timing and synchronization of different hardware components to ensure smooth running without delay [7].

A hardware design is an important module of the Zynq Board-based EVM, including the input modules such as button selections of a candidate for which voting is to be done, output modules such as LED displays giving an indication that the voting is confirmed, and storage modules where the voting data is stored securely. Description by Verilog explains the behavior of these modules and how they are related to each other [8]. The input module is intended to accurately capture and store voter choices, while the output module offers instant feedback to the voter in the form of confirmation of their vote. The storage module makes use of the internal memory of the Zynq Board to keep votes safely in a way that these cannot be changed or deleted without authorization [9].

Development of the EVM on the Zynq Board came in various stages. These include conceptual design and system architecture. A Verilog model was applied in modeling the system, and by simulating the voting logic, it becomes very easy to test and prove correctness. After successful simulation, a synthesis occurred whereby the design was implemented on the Zynq Board's FPGA fabric. The system was then tested quite strictly to validate the reliability and accuracy of the system across all conditions, such as high voter turnout and fault scenarios. Lastly, the system was subjected to security audits to identify all the vulnerabilities and mitigate them [10].

One of the biggest challenges in developing an EVM is to accommodate different electoral processes and laws. The EVM built with the Zynq board can accommodate multiple voting protocols including the single transferable vote, proportional representation, and first-past-the-post systems. With the modularity of the Verilog code, it is easily implemented and varied in its logic depending on the need of the election. This system can further be extended

with more sophisticated features like the recount ability after votes, audit trails, and voter verification mechanisms [11].

The provision of Verilog as part of the EVM design with Zynq Board brings in the efficient management of power since electronic voting machines are to be installed in places that may not have good power and may well be in remote or low-power surroundings. Here, then power consumption would need to be minimized as it does not necessarily have to affect performance. Low power circuit design is supported by Verilog wherein the FPGA fabric can be optimized to reduce its switching activity. In addition, the ARM processor on the Zynq Board supports multiple power modes to let the system get into a low power state in case it is not being used and hence extend the life of the machine's battery [12].

2 Literature Survey

One of the fields where research and development of a Zynq Board-Based Electronic Voting Machine (EVM) is developed using Verilog is the field of application in the embedded system domain so that an efficient and secure process of elections is maintained. Since the voting system is integrated and a critical application, it is very hard to integrate the feature of security into any such system, hence, the Zynq System-on-Chip (SoC) platform, which integrates programmable logic (FPGA) and a processing system (ARM processor), is an excellent choice to implement such a robust voting system [13]. This flexibility of the Zynq SoC in the integration of software and hardware functionalities allows it to be considered in real-time, high-performance systems such as EVMs. The implementation of Verilog as an HDL here guarantees efficient hardware-level programming and logic synthesis with obvious deterministic behavior in relation to voting systems [14].

On the other hand, the inherent microcontrollers or general-purpose processors that are utilized in traditional electronic voting systems are attractive and efficient but somehow hampered by their inflexibility, low security, and scalability [15]. The Zynq platform advances configurability because of the FPGA fabric utilized where designers can mold the hardware according to the specific security protocols applied, signal processing, and voting logic management. Since the design of the FPGA uses Verilog, the hardware resources are placed under tight control, which causes the machine to run with minimal latency and the optimal utilization of resources. Furthermore,

since Verilog can describe parallel operations, several voting processes can be carried on in parallel thus avoiding bottlenecks that would have resulted if voting happens in different places at peak time [16].

The most significant advantage of this design approach for the development of EVM with the Zynq platform is that it embeds a dual-core ARM Cortex-A9 processor. It is useful to include voter authentication and result computation and manage all data communications. Meanwhile, the FPGA fabric will then take charge of the time-critical functions implemented to achieve the determination of button press detection and voting signal processing [17]. The system will thus be improving in performance while at the same time being secure because the hybrid architecture isolates sensitive operations within the FPGA, thereby reducing the risk associated with software-based tampering [18].

The first issue to be addressed in the design of any voting system is security. To this effect, in the Zynq SoC, the direct implementation in the hardware of all cryptographic functions coupled with the ability to create custom-made modules for encryption using Verilog significantly increases the security of the system against hacking and intrusion. Additionally, reprogrammability in FPGAs makes the system adaptive against changing risks by changing its security attributes without calling for new hardware [19]. Therefore, the system would be able to adapt to varying electoral demands in terms of scale and context with the flexibility to fit into small-scale needs of local elections or even a national election vote [20].

3 Proposed System

The proposed system would be the Zynq Board-Based Electronic Voting Machine, designed and developed using Verilog. That would give more efficiency and security in voting processes. This system makes use of the ability of the Zynq-7000 series System on Chip (SoC), which contains both programmable logic with an FPGA, and a processing system with ARM Cortex-A9. It is a two-component combination, which accommodates the implementation of complicated hardware logic along with real-time processing, making it appropriate for the development of an electronic voting machine.

Two units that are mainly involved in the design of EVM systems are the control unit and the balloting unit. These units work to secure and make voting efficient.

The control unit: It is developed by using the ARM processor of the Zynq Board. Through this, the overall function of the EVM is controlled by the control unit. Here it would control how the users interact with it, process input from the voting buttons, and communicate with the other units. The voting procedure is also made more secure through the control unit, as each vote will be validated and undergo security protocols.

The balloting unit: It is developed with the FPGA fabric, there is where core voting logic is implemented. It will register the votes whenever a voter presses the button of a candidate. A state machine is applied to track the status of every vote, and the results are kept in a secure memory module. It's designed to vote quickly and without duplicates.

The design primarily went into two key parts: one is hardware implementation of voting logic using the FPGA fabric, and the other is software control for user interaction and result computation using the ARM processor. Voting logic was designed in the Verilog. In the designed circuitry, every candidate was provided with a button, and each push would generate a signal, which would then work in harmony with the use of a state machine implemented to keep track of the votes. After a vote had been cast, the system recorded the input and securely stored the data in a memory module. The processing capabilities of the Zynq board were tapped for displaying the results in an LCD display and for other features such as vote counting, candidate selection, and declaration of results.

Difficulties Found:

(1) **Hardware-Software Co-Design:** The two main problems were solving an efficient co-design of hardware and software so both the FPGA logic and ARM processors run together properly in the machine. It was necessary to synchronize the high-level C code with the low-level code generated for the processing unit on the Verilog code written for the FPGA.

(2) **Security Issues:** Data security and preventing multiple voting by the same user were significant issues. Secure storage systems, such as storing votes in tamper-proof storage, memory management, and vote encryption, played important roles.

In the case of the FPGA, there were strict timing constraints, such as in the voting logic; that is to say, a vote must be registered before it progresses, such that there is no delay when each vote is cast. It was challenging to balance this constraint during FPGA synthesis within the constraints of resource utilization.

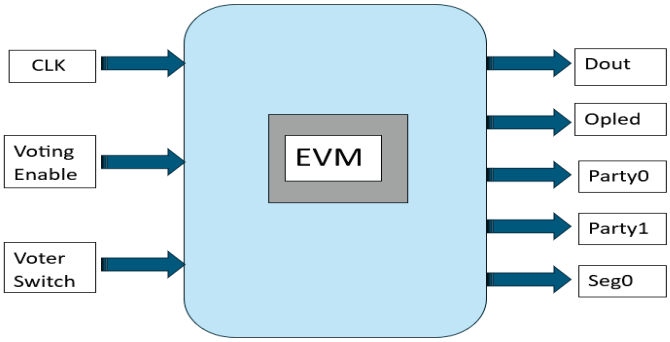

Figure 1 Modeling of EVM.

(3) **User Interface:** There was an absolute need to optimize the software running in the ARM core so that the user interface was intuitive and responsive. Their motto was that voter interaction with the system must be seamless and delay-free without errors. It has been tested and validated exhaustively at several stages of development. The model of the Verilog code was simulated with the ModelSim to ensure that the voting logic being implemented is correct, as well as the accuracy of vote counting. On the hardware side, the system was tested with real inputs on the Zynq board so all components of the system harmoniously worked together.

We tested the EVM functionally for accuracy in vote registration, handling multiple votes, and checking robustness in different scenarios such as power failure and reset. Further test cases involved boundary cases such as max voters' limits and the response of the system to simultaneous voting inputs.

To validate the security of voting, stress testing was conducted whereby a person should not be allowed to vote several times in favor of the same candidate.

Figure 1 shows the schematic of EVM with voting enable, clk, and voting switch. The structured approach would be to design and develop an EVM based on a Zynq Board using Verilog so that it can be implemented in an efficient manner and the working of the EVM is reliable. An EVM essentially should capture voter inputs, then store votes securely, and the vote should be rendered on the display in a user-friendly manner.

The approach starts with hardware design using Verilog. In developing, this approach has chosen Verilog specifically because it is one of the most

efficient tools for use in an FPGA platform like the Zynq Board to design digital logic circuits. A module is created to address key parts of the voting machine: voter input interface, vote counter, and result display. Each module is described in Verilog and then synthesized onto the programmable logic within the Zynq FPGA. We have paid special attention to debouncing the voting buttons' input signals so that the system does not count two votes for the same input due to signal noise.

The two major components of methodology are testing and validation. In this specific case, when we see the Verilog code, we first simulate it with tools like Xilinx Vivado to check for its logical correctness. Functional simulations would be carried out to check on all modules working properly. Once that passes, the design would then be synthesized and loaded to the Zynq Board. Then, hardware-in-the-loop testing was carried out, verifying if hardware and peripherals are interacting properly with each other and making sure that the system behaves correctly in the real world.

To add to that reliability, the electronic voting system design incorporates fault tolerance. An example would be the redundancy added to the vote counting and tallying where counters will cross-check the recorded votes; power-failure protection is also integrated into the system such that one can ensure the safe saving of the vote in case the system loses power. One method of ensuring this is through using non-volatile memory in keeping vote data.

Blockchain-based EVM solutions: It can change the face of electronic voting by introducing a decentralized and immutable ledger for recording votes. Every vote may then be retained as a unique encrypted block in the chain, thus tamper-proof in the virtual realm. It is open technology because any person with permission can verify the count for votes individually. This limits mistrust and fraud in elections. Blockchain further supports systems for remote voting, which have been proven effective and secure to hold verifiable elections to voters afar.

AI-driven systems: It is strong since it has a potent impact on the voting process because of improved verification of voters and helps in fraud detection as well. Due to the complexities of their algorithms, AI may thereby find voting behavior patterns and flag suspicious activities or breaches in real time. Biometric verification systems such as facial recognition or fingerprint scanning using AI would ensure that only legitimate voters cast their votes, further adding security. AI may thus further smoothen vote counting and aggregation and minimize human error to speed up election procedures.

4 Hardware Results

Hardware Results for the Design and Development of Zynq Board-Based Electronic Voting Machine Using Verilog: The hardware results reveal that the designed and developed system of a Zynq board-based electronic voting machine using Verilog was implemented and validated. For the hardware implementation, the main interest as well as the target was in obtaining the right performances from the election process, which is usually concerned with the capture of votes, the display of the results, and how the system reset for the next session of voting.

It utilized the Zynq-7000 SoC, which integrates FPGA fabric and ARM Cortex A9 processors. This was able to provide hardware-level voting functionality using synthesized and implemented Verilog code on the FPGA. While testing was in process, the voting machine had multiple voting buttons set up corresponding to different candidates. Votes for each candidate were counted, and no miscount was added to the system. The output is displayed on a seven-segment display or an LCD screen, as opted for. With the help of Verilog, voting logic is designed such that it processes the inputs from the buttons, records the votes, and ensures one does not vote again with debouncing techniques to remove wrong inputs from the buttons.

To ensure a safe and reliable vote, reset functionality was included. After the vote was accomplished, the reset button cleared the previous votes and got the system ready for the next voting session. An authentication mechanism for voters using an external module was included to demonstrate that the design can be extended to support authentication in the next iteration, secure.

Blockchain-based voting systems: It could further innovation, reaching unparalleled security and transparency. With a decentralized and immutable ledger, blockchain can secure the recording of votes so that each vote may be stored cryptographically and then verified by any party interested in verifying it; any form of corruption or fraud is thus impossible. This also supports remote voting, whereby people can securely place a ballot from anywhere in the world, opening up access for previously disenfranchised populations.

Figure 2, shows an EVM, with a ‘press of a button’ registration of a vote, with many buttons inside this control panel representing various candidates. One button inside the control panel is pressed, in a color that is brighter than the other buttons to indicate that it is currently being activated. Above the buttons is the small digital display that says “Vote Logged” as recognition of the event, and next to that is a timer countdown saying “Sufficient Time” for another vote to be submitted, thus eliminating fast, repeated entries.

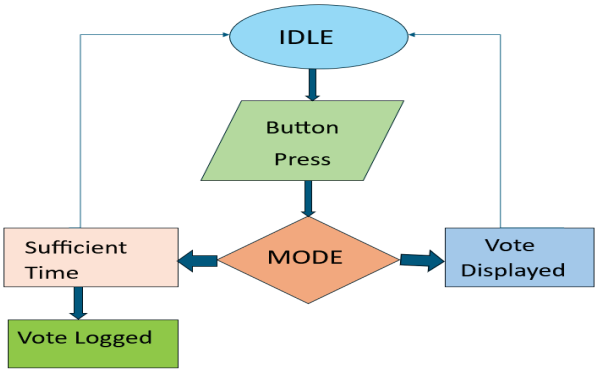

Figure 2 Display of the control panel.

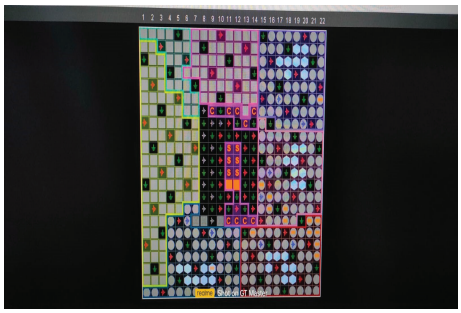

Figure 3 Synthesis of control access.

Figure 3 shows the synthesis of the ZedBoard in Verilog shown below, and the amount of detail involved in this process is evident from the image. The layout therefore shows a graphical version of the synthesized design, including flip-flops, lookup tables (LUTs), and interconnections.

Figure 4 shows a picture of a ZedBoard, one kind of development board for the Zynq-7000 SoC, kept on a workbench before implementing an EVM with Verilog. Connectors and peripherals abound on the ZedBoard, including GPIO pins, a USB interface, and an HDMI port.

Figure 5 shows the insertion of the Verilog code also appears as the image symbolically represented by an overlay of a code snippet or abstract graphic representing the operation of the hardware based on the same programmatic logic; the hardware and software implementation are connected, thereby showing the technological innovation within the current elections. The image, therefore, represents the underlying principle behind the secure and efficient mechanism for voting granted by advanced electronics and programming.

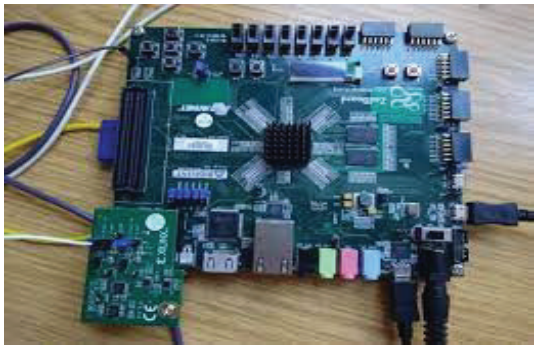

Figure 4 Devlopment of Zedboard for testing.

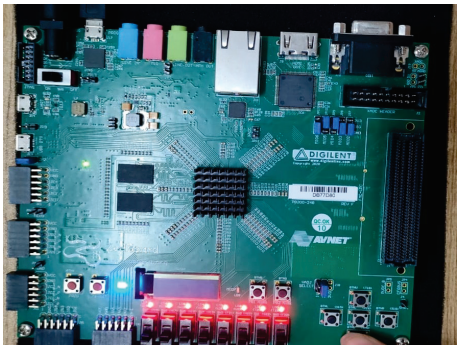

Figure 5 Device before the vote validation.

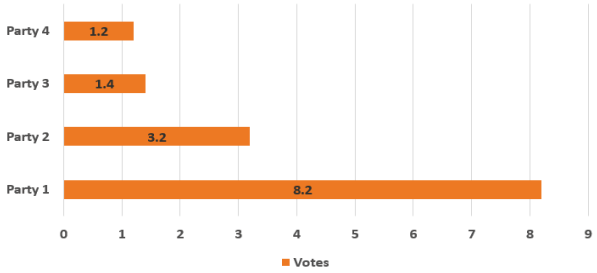

Figure 6 Representation of Votes for various parties.

Figure 6 the above graph represents the voting setup in an electronic voting machine that shows the voting process of different political parties. The vertical axis represents the number of votes, and the horizontal axis represents several political parties. A different bar or segment is drawn on

the graph for each party but colored differently so as to better distinguish between them.

5 Conclusion

From the above discussions, the designing and developing EVM based on the Zynq Board describe successfully that the creation of an electronic voting machine is straightforward with the given premise of security, reliability, and efficiency in digital voting. The exploration results of the present project described that by utilizing the dual capability of the Zynq platform – FPGA and software-driven processing – it is truly possible to overcome most of the challenges made by voting methods from time immemorial. The high accuracy of vote control through Verilog ensures proper casting and counting of votes, eliminating chances of error or security breaches. There is flexibility in FPGA, which provides resistance to tampering and offers very high-speed processing, ideal for large-scale elections demanding high throughput and security.

The most important finding was that of an obvious advantage in the use of FPGA-based systems for environments requiring secure electronic voting. The hardware acceleration aspect of the Zynq platform improved the system performance offloading critical and resource-demanding tasks such as vote logging and ballot validation onto the FPGA, while the ARM processor takes care of the rest about user interface and result computations.

References

[1] J. M. Bohli, C. Henrich, C. Kempka, J. Muller-Quade and S. Rohrich, "Enhancing Electronic Voting Machines on the Example of Bingo Voting," in *IEEE Transactions on Information Forensics and Security*, vol. 4, no. 4, pp. 745–750, Dec. 2009.

[2] A. Villafiorita, K. Weldemariam and R. Tiella, *Development, Formal Verification, and Evaluation of an E-Voting System With VVPAT* in IEEE Transactions on Information Forensics and Security, vol. 4, no. 4, pp. 651–661, Dec. 2009.

[3] R. A. Fink, A. T. Sherman and R. Carback, "TPM Meets DRE: Reducing the Trust Base for Electronic Voting Using Trusted Platform Modules," *IEEE Transactions on Information Forensics and Security*, in vol. 4, no. 4, pp. 628–637, Dec. 2009.

[4] S. Raut, V. Talekar and A. Govardhan, "Digital Electronic Voting Machine Using Raspberry Pi and Touchscreen Display," 2021 5th *International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT)*, pp. 752–756, 2021.

[5] M. R. Alam, M. Masum, M. Rahman and A. Rahman, "Design and implementation of microprocessor based electronic voting system," 2008 11th *International Conference on Computer and Information Technology*, Khulna, Bangladesh, pp. 264–269, 2008.

[6] R. Rezwan, H. Ahmed, M. R. N. Biplob, S. M. Shuvo and M. A. Rahman, "Biometrically secured electronic voting machine," 2017 *IEEE Region 10 Humanitarian Technology Conference (R10-HTC)*, 2017.

[7] B. N. K. Reddy, M. Zia Ur Rahman and A. Lay-Ekuakille, "Enhancing Reliability and Energy Efficiency in Many-Core Processors Through Fault-Tolerant Network-on-Chip," in *IEEE Transactions on Network and Service Management*, vol. 21, no. 5, pp. 5049–5062, 2024.

[8] D. A. Kumar and T. U. S. Begum, "Electronic voting machine – A review," *International Conference on Pattern Recognition, Informatics and Medical Engineering (PRIME-2012)*, pp. 41–48, 2012.

[9] V. K. Priya, V. Vimaladevi, B. Pandimeenal and T. Dhivya, "Arduino based smart electronic voting machine," 2017 *International Conference on Trends in Electronics and Informatics (ICEI)*, pp. 641–644, 2017.

[10] A. BalaMurali, P. S. Sravanthi and B. Rupa, "Smart and Secure Voting Machine using Biometrics," 2020 *Fourth International Conference on Inventive Systems and Control (ICISC)*, pp. 127–132, 2020.

[11] Govindaraj, Ramya, and P. Kumaresan. "Online Voting System using Cloud." 2020 International Conference on Emerging Trends in *Information Technology and Engineering (ic-ETITE).* IEEE, 2020.

[12] B. N. K. Reddy, S. Jogi and S. K, "Design and Implementation of an FPGA-based Emulator Circuit for MLP using Memristors," 2024 28th *International Symposium on VLSI Design and Test (VDAT)*, pp. 1–6, 2024.

[13] Bhuvana Priya, R., P. Sivapriya, and V. K. G. Kalaiselvi. "*Smart voting*." 2017 2nd International Conference on Computing and Communications Technologies (ICCCT). IEEE, 2017.

[14] Avinash, N. J., et al. "High Performance Electronic Voting Machine (EVM) Implementation Using ARM Cortex M3." 2020 Fourth International Conference on I-SMAC (IoT in Social, Mobile, Analytics and Cloud)(I-SMAC). IEEE, 2020.

[15] Ali, Sahibzada Muhammad, et al. "Micro-controller based smart electronic voting machine system." IEEE International Conference on Electro/Information Technology. IEEE, 2014.
[16] S. Yadav, Punith, M.S., Shukla, R., "Blockchain based Electronic Voting Machine" International Conference on Edge Computing and Applications, pp. 479–483, 2022.
[17] Giordano, R., Barbieri, D., Perrella, S., Tortone, G., Di Capua, F., Aloisio, A. (2018, November). Beam and Field Testing of Configuration Self-repair in Xilinx FPGAs. In 2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC), pp. 1–2, 2018.
[18] G. S. Reddy, S. Radha, K. T. Taufiq, K. D. S. Reddy, K. P. K. Reddy and P. Nagabushanam, "Security based Electronic Voting Machine using Xilinx tool," 2022 2nd International Conference on Power Electronics & IoT Applications in Renewable Energy and its Control (PARC), pp. 1–4, 2022.
[19] R. Pezzuol Jacobi, F. Trindade, J. Porfirio A. de Carvalho and R. Cantanhede, "JPEG decoding in an electronic voting machine," *Proceedings 13th Symposium on Integrated Circuits and Systems Design* (Cat. No. PR00843), pp. 177–182, 2000.
[20] Singh, A., Yadav, A., Kumar, A., Singh, K. "A Review of Smart Electronic Voting Machine," hird International Conference on Sustainable Computing. *Advances in Intelligent Systems and Computing*, vol. 1404. Springer, 2022.

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